

302,032

FIG. 1

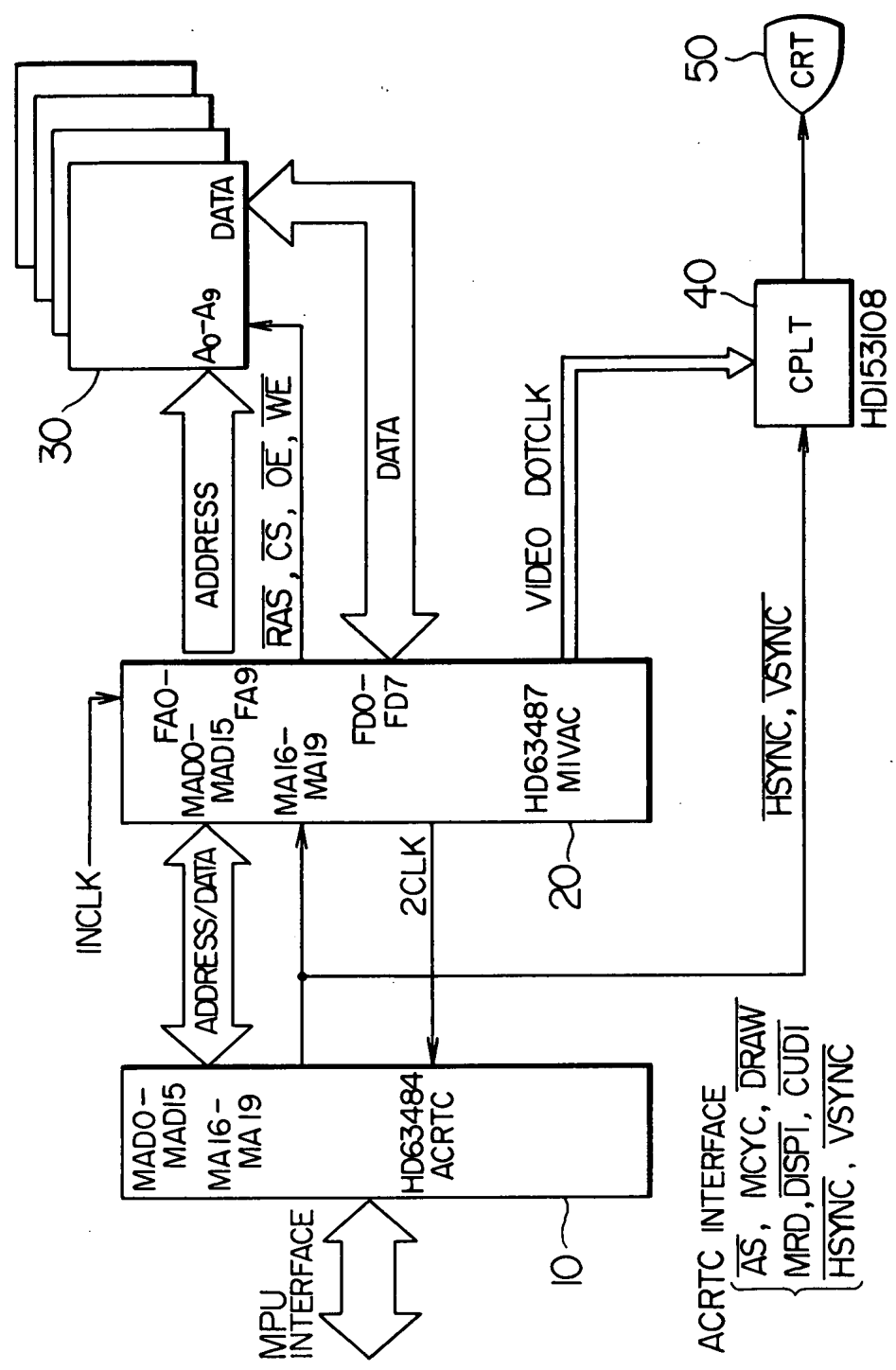


FIG. 2

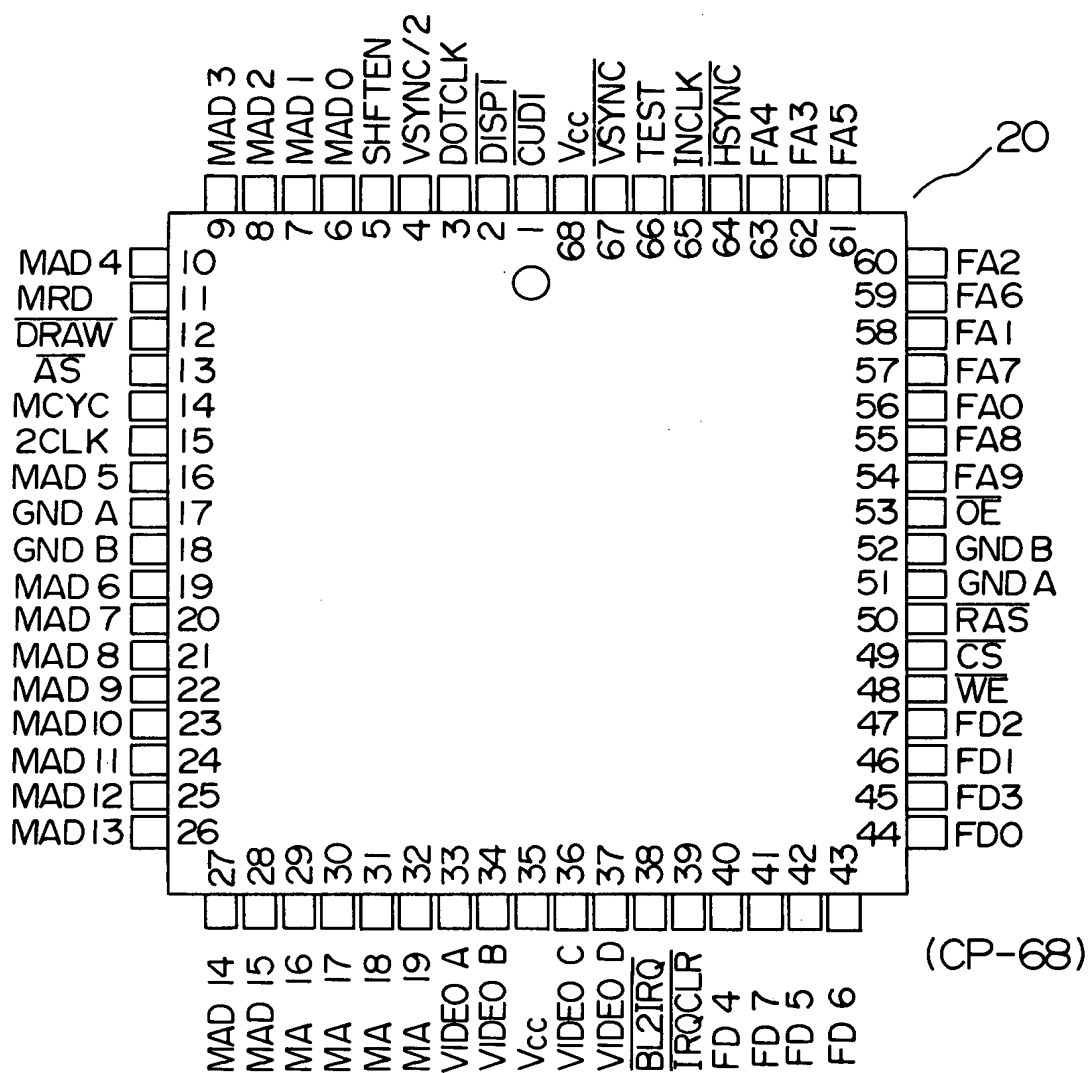


FIG. 3a

ITEM	TERMI- NAL NO.	TERMI- NAL NAME	INPUT/ OUTPUT	FUNCTION
POWER SUPPLY	35,68	Vcc	—	+ 5V IS SUPPLIED.
	17,18 51,52	Vcc	—	GND IS CONNECTED.
OPERATION CONTROL SIGNAL	65	INCLK	INPUT	BASIC CLOCK OF MIVAC IS INPUTTED.
	66	TEST	INPUT	MIVAC OPERATION IS TESTED. SET THIS TERMINAL TO "LOW" LEVEL.
ACRTC INTERFACE SIGNAL	15	2CLK	OUTPUT	2CLK SIGNAL IS SUPPLIED TO ACRTC. THIS SIGNAL IS ASYMMETRIC, NAMELY, HAS DIFFERENT CYCLE LENGTHS IN THE FIRST HALF AND SECOND HALF OF A MEMORY CYCLE.
	14	MCYC	INPUT	MCYC SIGNAL FROM ACRTC IS INPUTTED. MCYC INDICATES "LOW" AND "HIGH" LEVELS WHEN ACRTC IS IN ADDRESS AND DATA CYCLES, RESPECTIVELY.
	12	DRAW	INPUT	DRAW SIGNAL FROM ACRTC IS INPUTTED. DRAW INDICATES WHETHER OR NOT ACRTC IS IN THE DRAW CYCLE. DRAW IS "LOW" LEVEL IN THE DRAW CYCLE AND IS "HIGH" LEVEL IN THE OTHER CYCLES.
	11	MRD	INPUT	MRD SIGNAL FROM ACRTC IS INPUTTED. MRD CONTROLS DATA TRANSFER DIRECTION BETWEEN FRAME BUFFER AND ACRTC. WHEN DATA IS READ FROM FRAME BUFFER, "HIGH" LEVEL IS INPUTTED. WHEN DATA IS WRITTEN IN FRAME BUFFER, "LOW" LEVEL IS INPUTTED.
	13	$\overline{AS}$	INPUT	$\overline{AS}$ SIGNAL IS INPUTTED FROM ACRTC $\overline{AS}$ INDICATES PRESENCE OR ABSENCE OF MEMORY ACCESS.
	64	$\overline{HSYNC}$	INPUT	HSYNC SIGNAL IS INPUTTED FROM ACRTC. UNDER CONDITIONS OF $\overline{HSYNC}$ = "LOW" AND $\overline{DRAW}$ = "HIGH", IF AS PULSE IS RECEIVED, $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH OPERATION IS CARRIED OUT.
	67	$\overline{VSYNC}$	INPUT	$\overline{VSYNC}$ SIGNAL IS INPUTTED FROM ACRTC. RECEIVED $\overline{VSYNC}$ IS DIVIDED BY TWO SO AS TO OUTPUTTED AS $\overline{VSYNC}/2$ SIGNAL AND IS ALSO USED TO CONTROL MULTIPLEXER OF VIDEO OUTPUT.
	2	$\overline{DISP1}$	INPUT	$\overline{DISP1}$ SIGNAL IS INPUTTED FROM ACRTC. $\overline{DISP1}$ INDICATES SCREEN DISPLAY PERIOD. ORDINARILY, SET "1" TO DISPLAY SIGNAL CONTROL (DSC) BIT OF ACRTC.
	1	$\overline{CUD1}$	INPUT	$\overline{CUD1}$ SIGNAL IS INPUTTED FROM ACRTC. $\overline{CUD1}$ IS LOADED WITH "LOW" LEVEL DURING GRAPHIC CURSOR DISPLAY PERIOD.
	6-10 16 19-28	MADO -MAD15	INPUT/ OUTPUT	MODE-MAD15 OF ACRTC ARE INPUTTED. THESE SIGNALS ARE USED AS FRAME BUFFER ACCESS ADDRESS IN ADDRESS CYCLE FOR MCYC = "LOW", AS DATA INPUT/OUTPUT FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER IN DATA TRANSFER CYCLE FOR MCYC = "HIGH".
	29-32	MA16- MA19	INPUT	FRAME BUFFER ACCESS ADDRESS MA16 - MA19 IS INPUTTED FROM ACRTC.

FIG. 3b

ITEM	TERMI- NAL NO.	TERMI- NAL NAME	INPUT/ OUTPUT	FUNCTION
FRAME BUFFER INTERFACE SIGNAL	50	RAS	OUTPUT	RAS TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	49	CS	OUTPUT	CS TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	48	WE	OUTPUT	WE TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	53	OE	OUTPUT	OE TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	56,58 60,62 63,61 59,57 55,54	FA0 - FA 9	OUTPUT	MULTIPLEX ADDRESS IS OUTPUTTED FOR DRAM. ADDRESS TO BE MULTIPLEXED VARIES DEPENDING ON VCF0-VCF3 AND VMD0 ATTRIBUTE CODES.
	44,46 47,45 40,42 43,41	FDO - FD7	INPUT/ OUTPUT	FD IS 8-BIT INPUT/OUTPUT SIGNAL FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER AND FOR FETCHING DISPLAY DATA READ FROM FRAME BUFFER. IN A CASE OF ONE MEMORY CHIP, FD0-FD3 ARE USED, WHEREAS IN A CASE OF TWO FOUR MEMORY CHIPS, FD0-FD7 ARE USED.
CRT DISPLAY INTERFACE SIGNAL	3	DOTCLK	OUTPUT	DOTCLK SIGNAL IS DELIVERED BY DIVIDING INCLK SIGNAL AS BASIC INPUT SIGNAL OF MIVAC BY 1, 2 OR 4. DIVISION RATIO IS SET DEPENDING ON VCF0-VCF3 OF ATTRIBUTE CODE.
	33, 34 36, 37	VIDEO A -VIDEO D	OUTPUT	VIDEO A-D SIGNAL IS 4-BIT OUTPUT SIGNAL WHICH IS OBTAINED BY CONVERTING DISPLAY DATA FROM PARALLEL SIGNAL INTO SERIAL SIGNAL BY SHIFT REGISTER OF MIVAC AND WHICH IS DELIVERED DURING DISPLAY PERIOD INDICATED BY SHFTEN OUTPUT. 4-BIT VIDEO SIGNAL IS DETERMINED BY ATTRIBUTE CODE VCF0-VCF3.
	5	SHFTEN	OUTPUT	SHFTEN INDICATES DISPLAY PERIOD OF VIDEO SIGNAL AND IS SET TO "HIGH" LEVEL DURING DISPLAY PERIOD. IN SINGLE ACCESS, DISP1 FROM ACRTC IS ELONGATED BACKWARD BY ONE CYCLE, AND IN DUAL ACCESS, DISP1 IS ELONGATED BACKWARD BY TWO CYCLES SO AS TO PRODUCE THIS SIGNAL.
	4	VSNC/2	OUTPUT	VSNC/2 SIGNAL IS INPUTTED TO ACRTC. VSNC IS DIVIDED BY TWO FOR PRODUCING THIS SIGNAL.
OTHERS	38	BL2IRQ	OUTPUT	BL2IRQ IS SET BY BLINK2(MA19) INPUTTED IN ATTRIBUTE CYCLE. DURING ATTRIBUTE CYCLE, WHEN BLINK2 IS AT "HIGH" LEVEL, BL2IRQ IS SET TO "LOW" LEVEL.
	39	IRQCLR	INPUT	IRQCLR SIGNAL IS USED TO CLEAR BL2IRQ SIGNAL. WHEN "LOW" IS INPUTTED TO IRQCLR, BL2IRQ IS CLEARED TO "HIGH" LEVEL.

FIG. 4

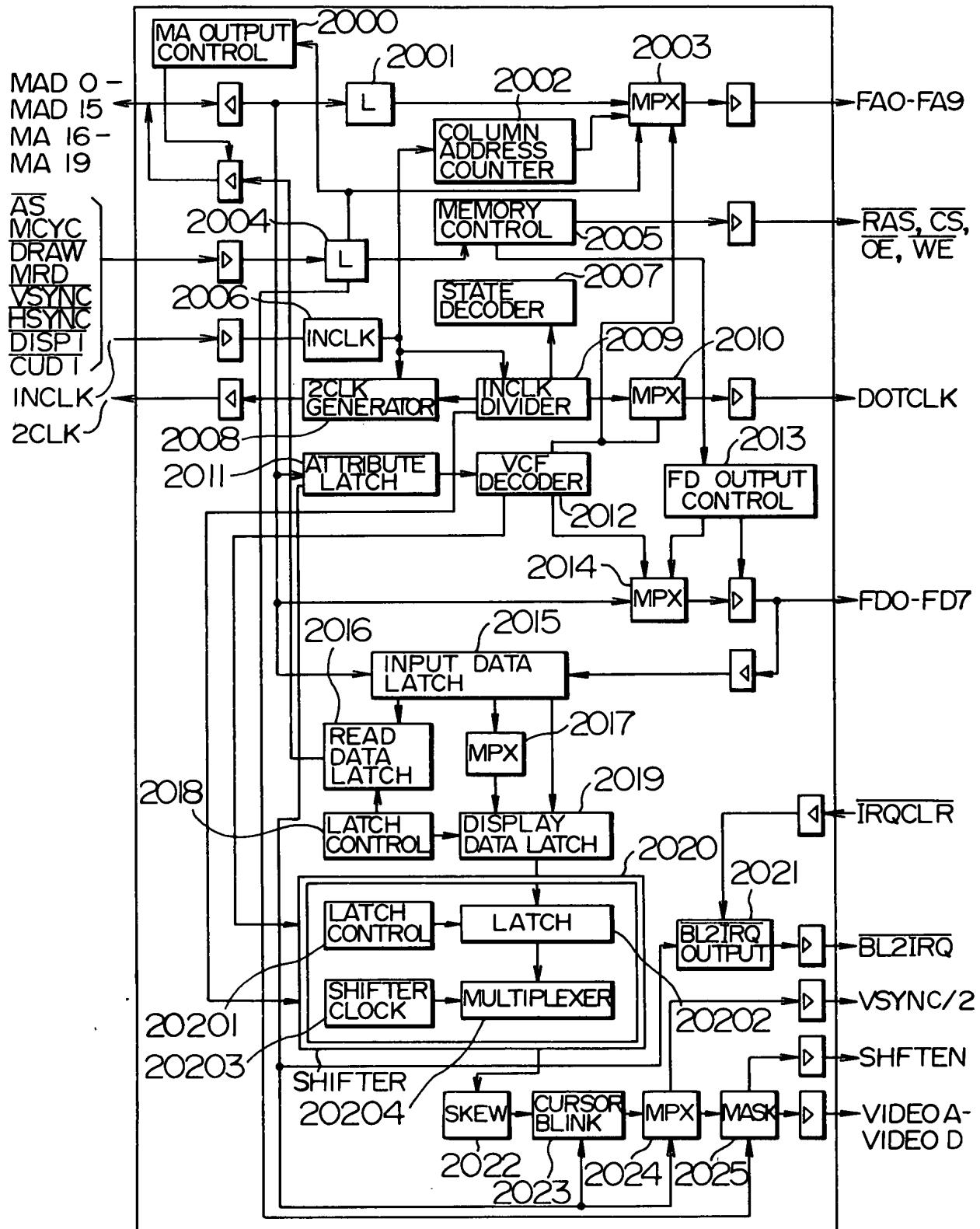


FIG. 5a

1-CHIP MEMORY

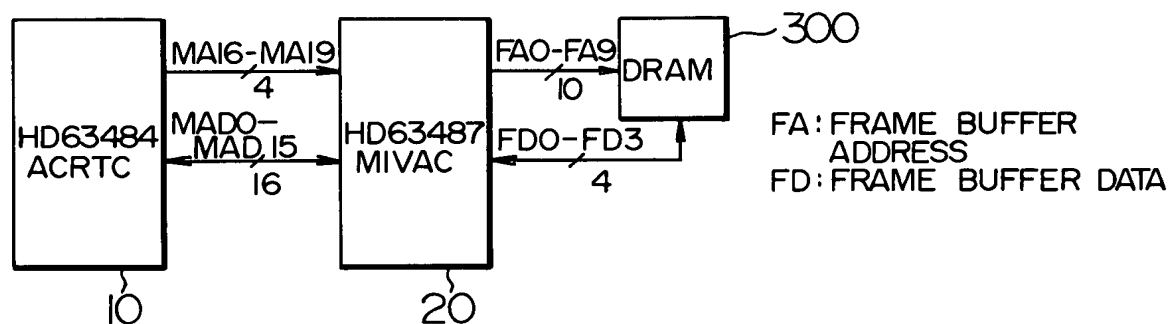


FIG. 5b

2-CHIP MEMORY

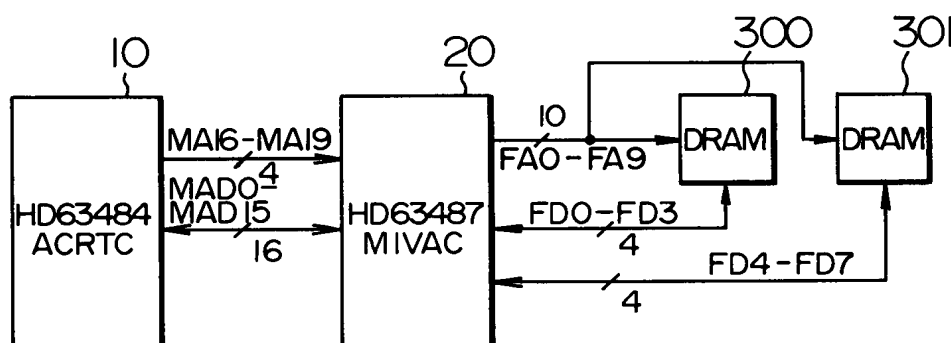


FIG. 5c

4-CHIP MEMORY

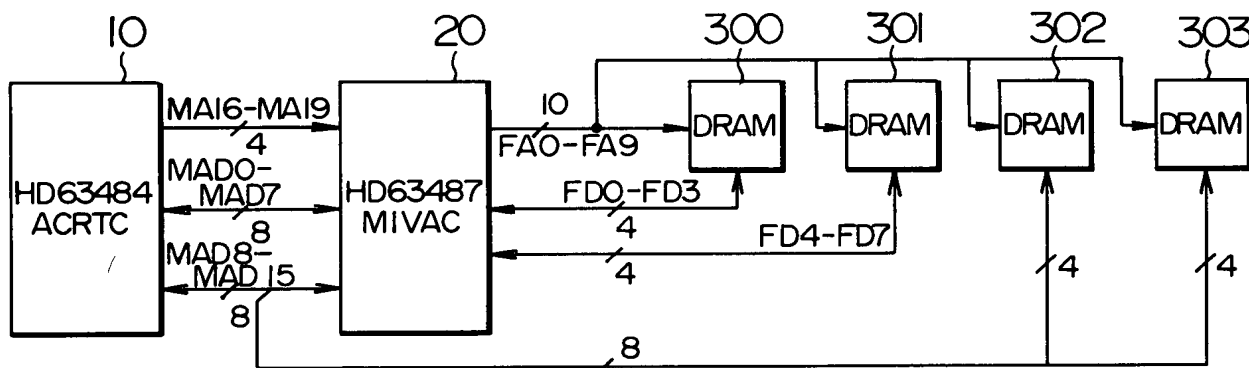


FIG. 6

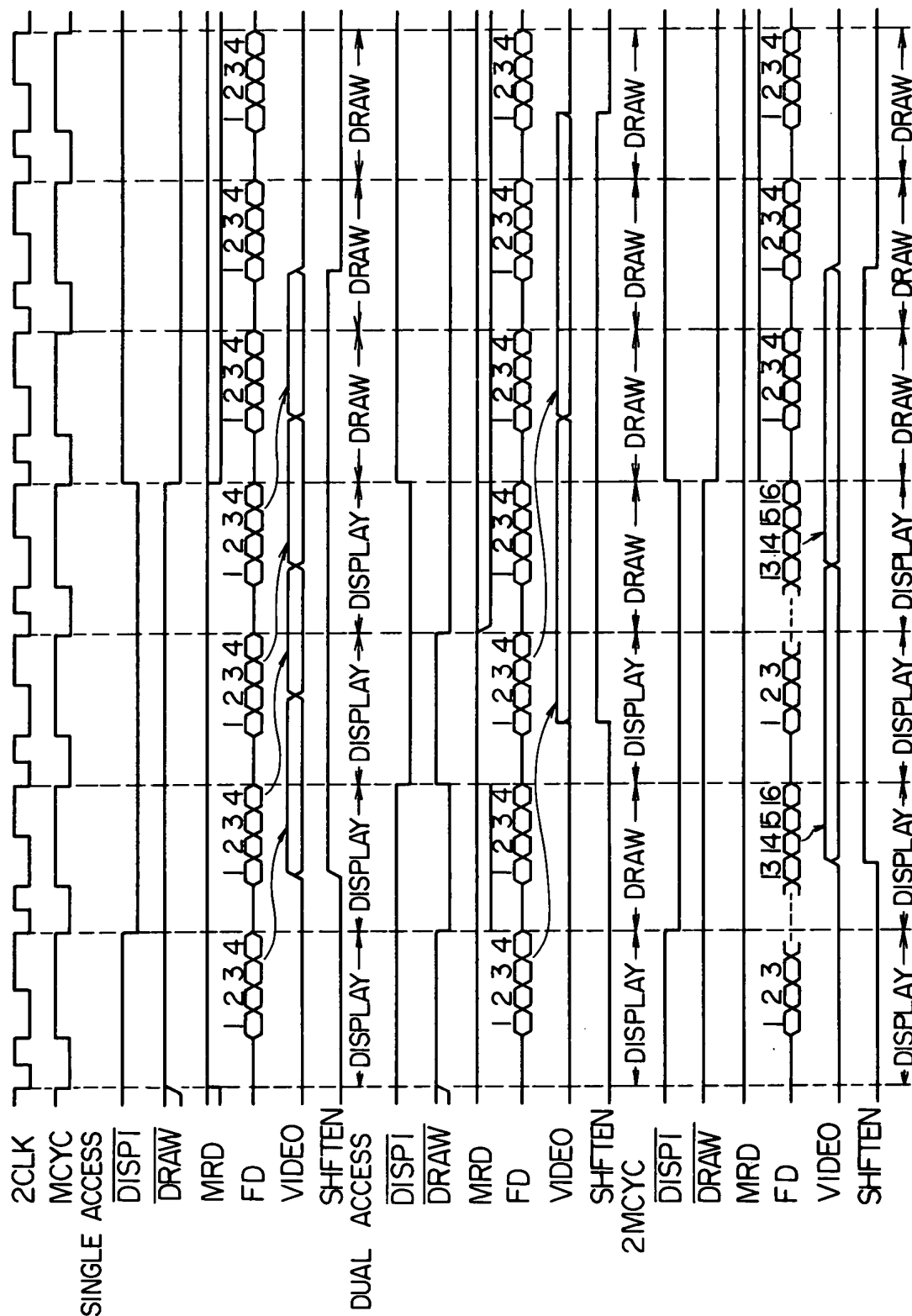


FIG. 7

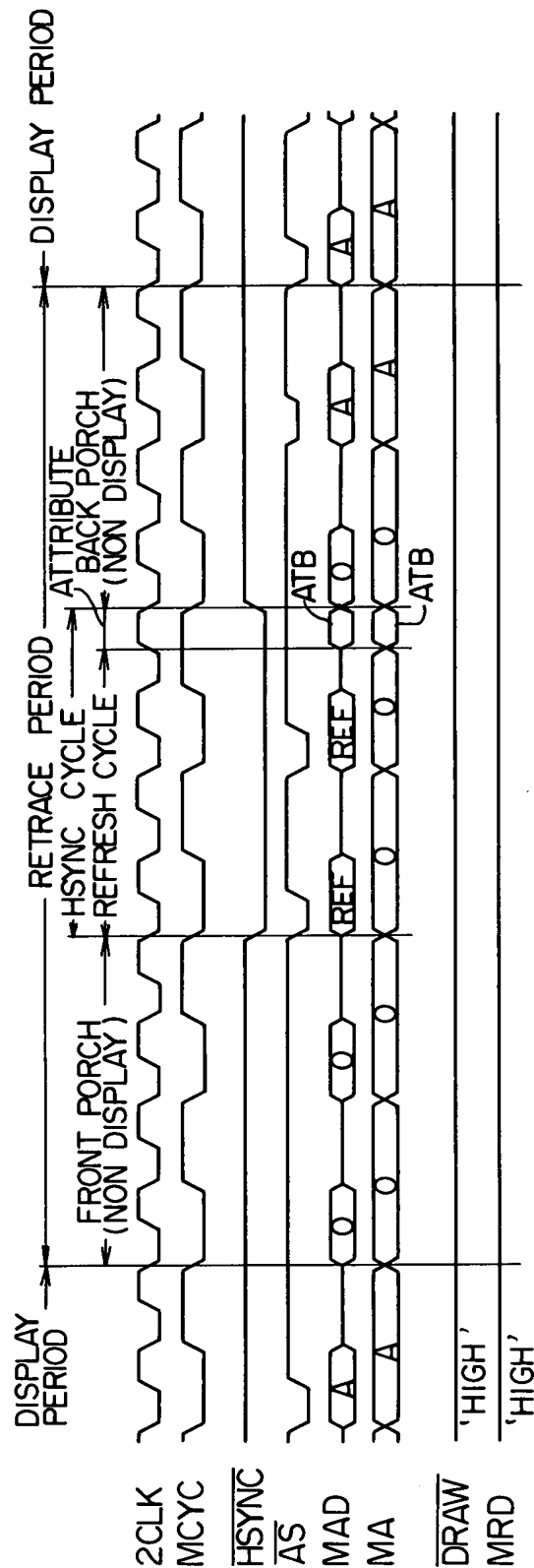


FIG. 11

CUR I	CUR O	CURSOR DISPLAY COLOR
0	0	BLACK ( VIDEO A - VIDEO D = 0 )
0	1	WHITE ( VIDEO A - VIDEO D = 1 )
1	0	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO D
1	1	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO C (VIDEO D IS KEPT UNCHANGED)



FIG. 8

MA19	BLINK 2	BL2IRQ OUTPUT IS SET
MA18	BLINK 1	BLINKING OF GRAPHIC CURSOR IS SET
MA17	SPL 2	
MA16	SPL 1	
MAD15	HZ 3	
	}	
MAD12	HZ 0	NOT USED IN MIVAC
MAD11	HSD 3	
	}	
MAD 8	HSD 0	
MAD 7	MUXEN	MULTIPLEXING OF VIDEO OUTPUT IS SET
MAD 6	VMD	DEPTH OF FRAME BUFFER MEMORY IS SET
MAD 5	CUR 1	
MAD 4	CUR 0	DISPLAY COLOR OF GRAPHIC CURSOR IS SET
MAD 3	VC F 3	
MAD 2	VC F 2	OPERATION MODE (DISPLAY COLOR, SHIFT AMOUNT OF
MAD 1	VC F 1	SHIFT REGISTER, ACCESS MODE, ETC.) OF MIVAC IS SET
MAD 0	VC F 0	

FIG. 9

MODE	CRT SCREEN LAYOUT EXAM- PLE (DOTS X RASTER)	MAXIMUM FRAME BUFFER CA- PACITY (BYTES)	ACRTC OP- ERATION FREQUENCY (MHz)	MEMORY ACCESS SPEED	HIGH- SPEED DRAWING	NUMBER OF MEMO- RIES	COLOR/ GRADA- TION	SHIFT AMOUNT (BITS)	MAXIMUM DOT CLOCK FREQ. (MHz)
0	640x200, 350, 400, 480		4.13	480 ns/ 4ACCESSES	—	1		16	33
1	640x200, 480x240, 320x200, 240	512K/128K					4	8	16.5
2	320x200, 240 266x192						16	4	8.25
3	640x200, 350, 400, 480					2	4	16	33
4	640x200, 480x240, 320x200, 240	1M/256K					16	8	16.5
5	640x200, 350, 400, 480	2M/512K				4			33
6	640x200, 480x240, 320x200, 240	512K/128K				1		16	16.5
7	320x200, 240 256x192						4	8	8.25
8	640x200, 350, 400, 480					2		32	33
9	640x200, 480x240, 320x200, 240	1M/256K					4	16	16.5
A	320x200, 240 256x192						16	8	8.25
B	640x200, 350, 400, 480					4	4	32	33
C	640x200, 480x240, 320x200, 240	2M/512K					16	16	16.5
D	640x200, 350, 400, 480					1	4	32	33
E	640x200, 480x240, 320x200, 240	512K/128K					16	16	16.5
F	640x200, 350, 400, 480	1M/256K		960ns/ 16ACCESSES	—	2		32	33

F I G. 10

MODE	DOT CLOCK FREQUENCY
0, 3, 5, 8 B, D, F	33MHz ~ 11MHz
1, 4, 6, 9 C, E	16.5MHz ~ 5.5MHz
2, 7, A	8.25MHz ~ 2.75MHz

F I G. 12

VMD	MEMORY CHIP EMPLOYED
0	256 K × 4 BIT DRAM
1	1 M × 4 BIT DRAM

F I G. 13

MUXEN	VSNC / 2	VIDEO A	VIDEO B
0	0	A	B
	1	A	B
1	0	A	B
	1	C	D

F I G. 14

BLINK I	GRAPHIC CURSOR DISPLAY
0	NOT DISPLAYED
1	DISPLAYED

FIG. 15a

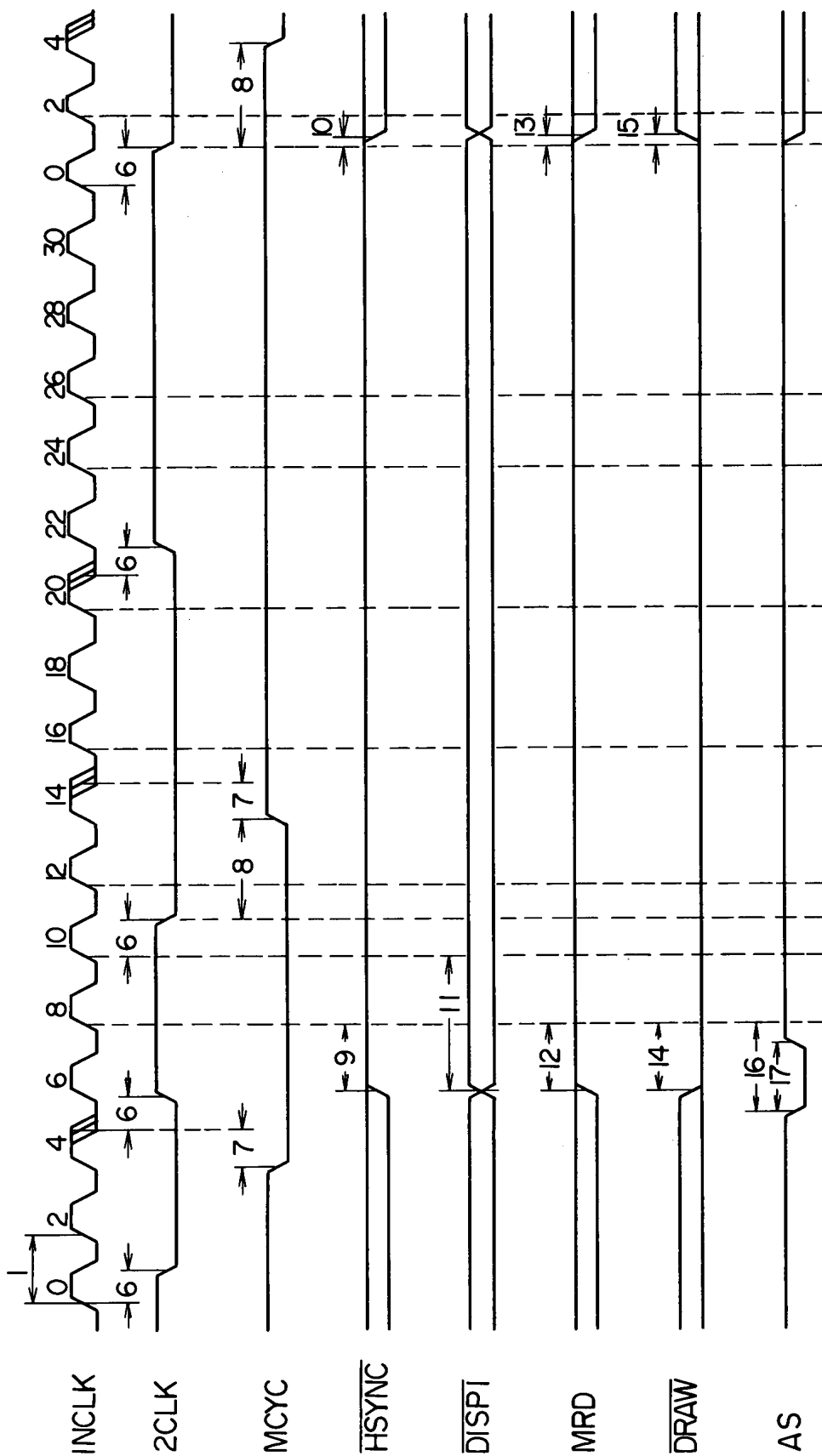


FIG. 15b

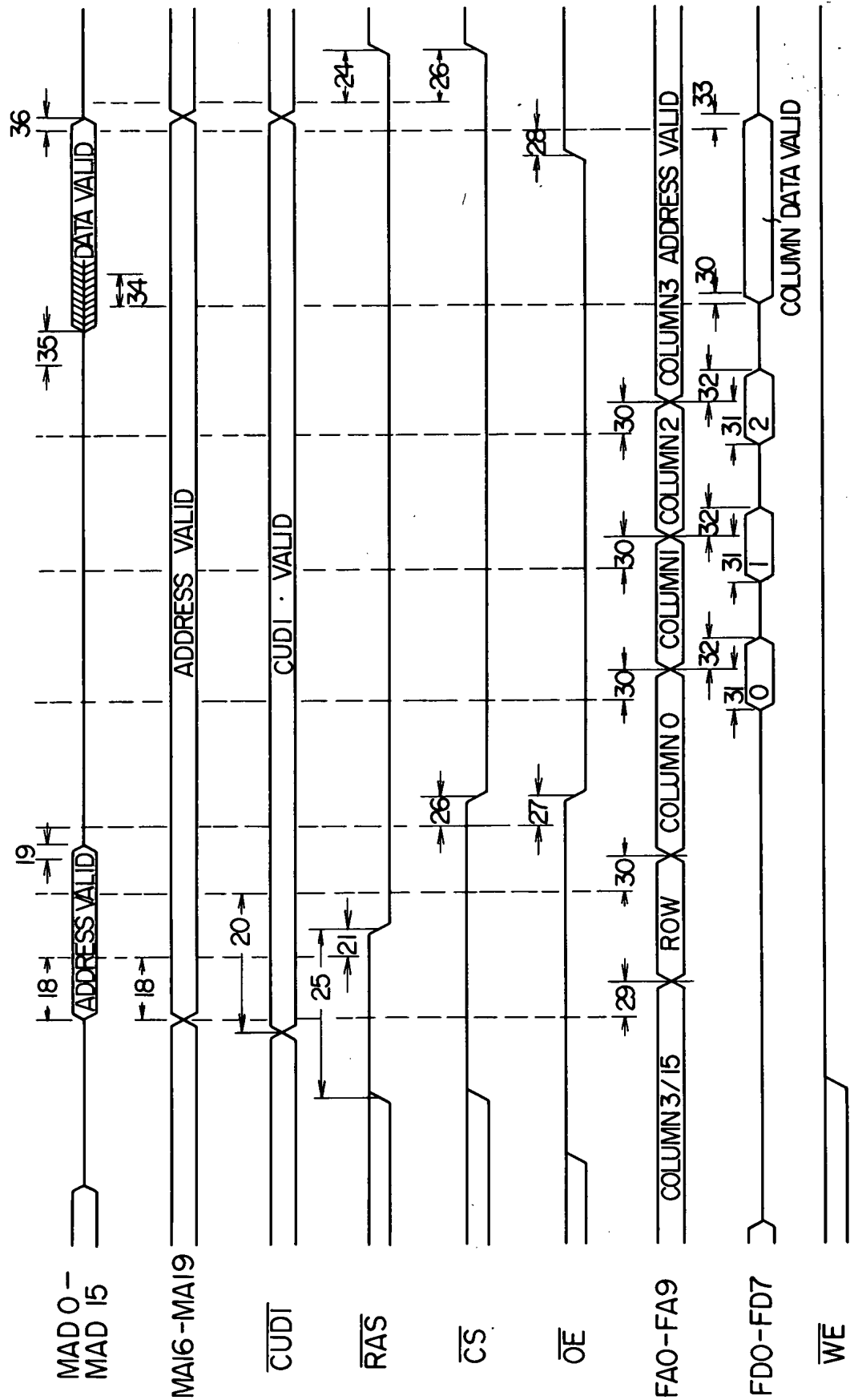
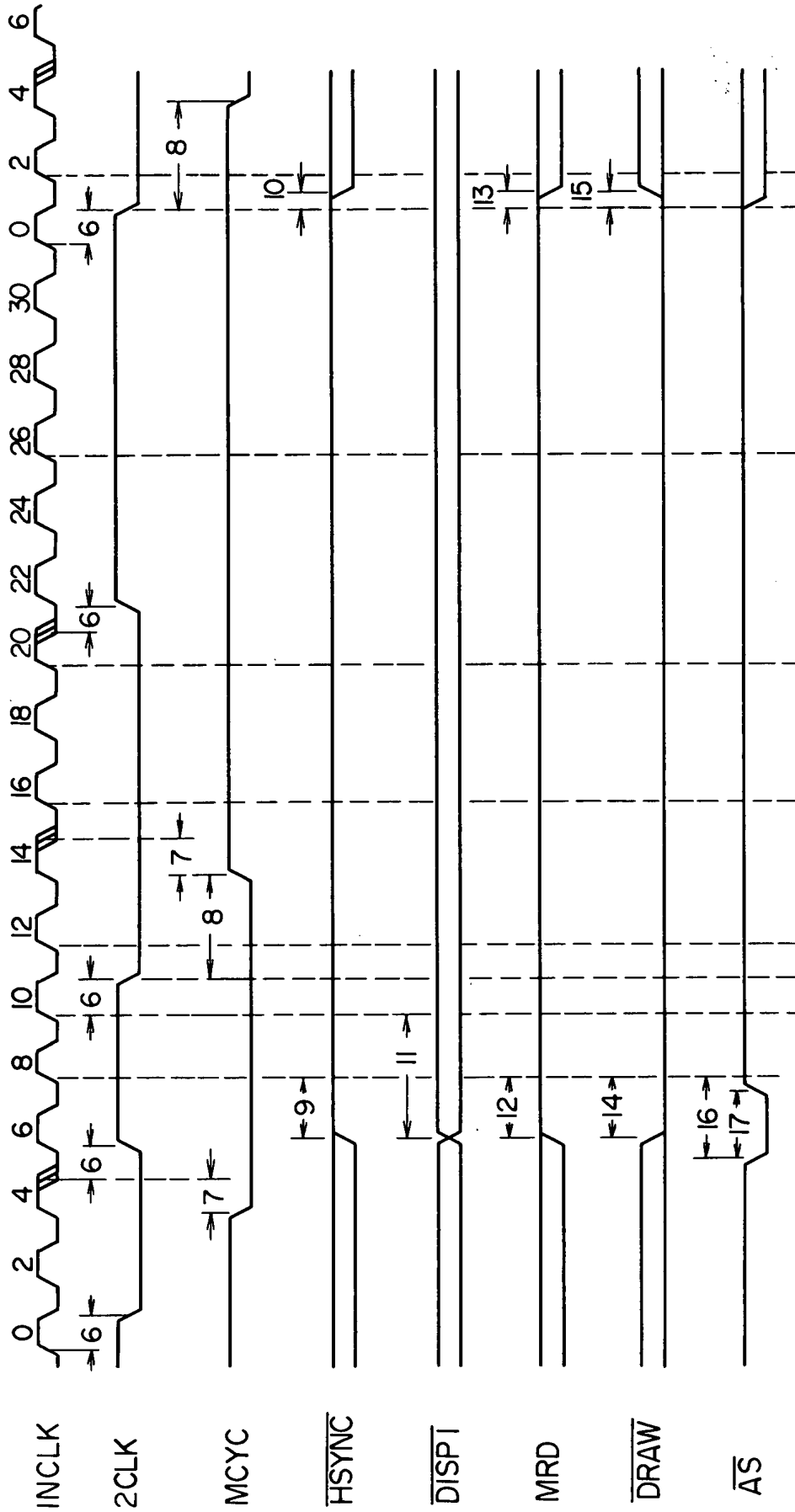


FIG. 16a



**F I G. 16b**

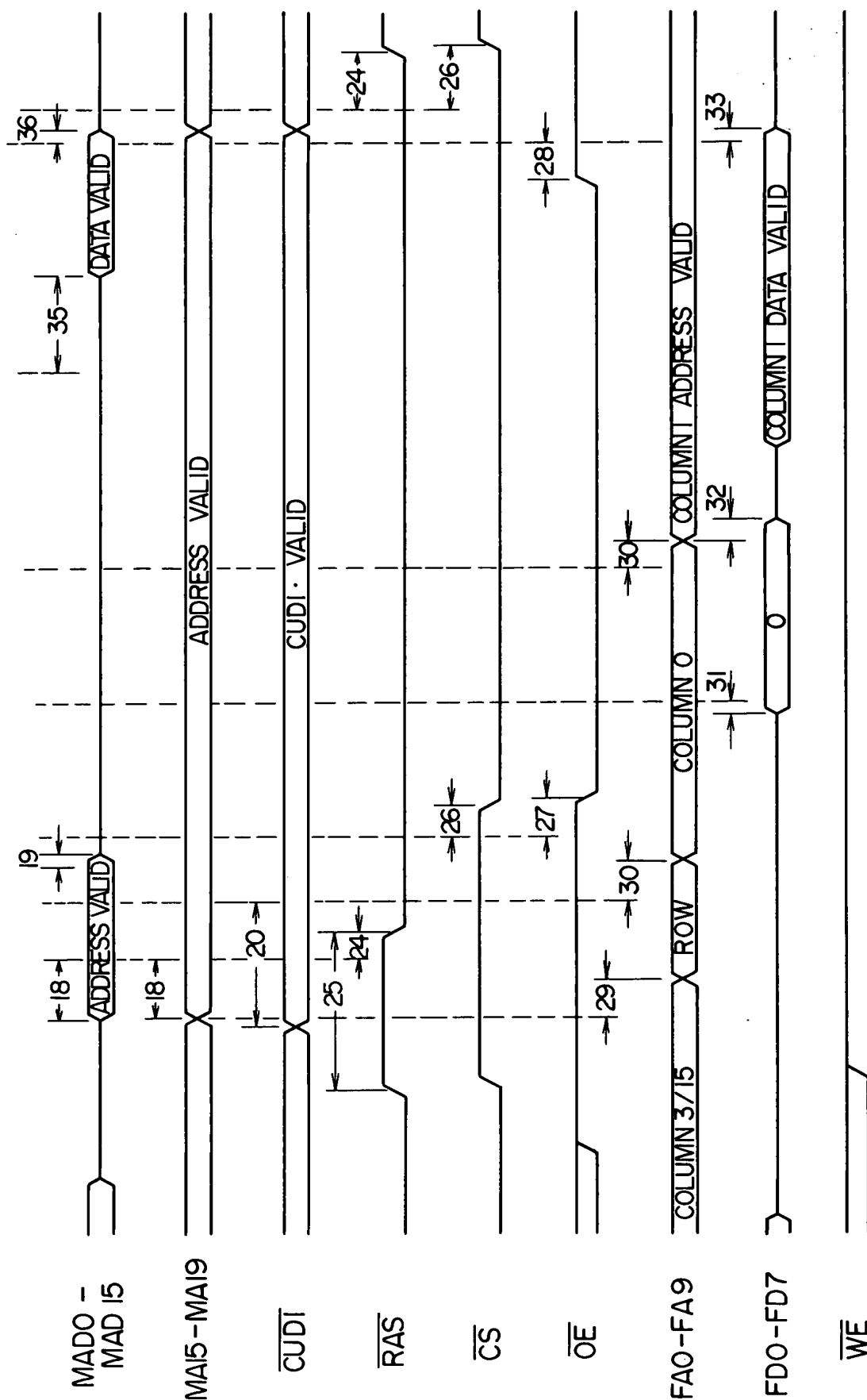


FIG. 17a

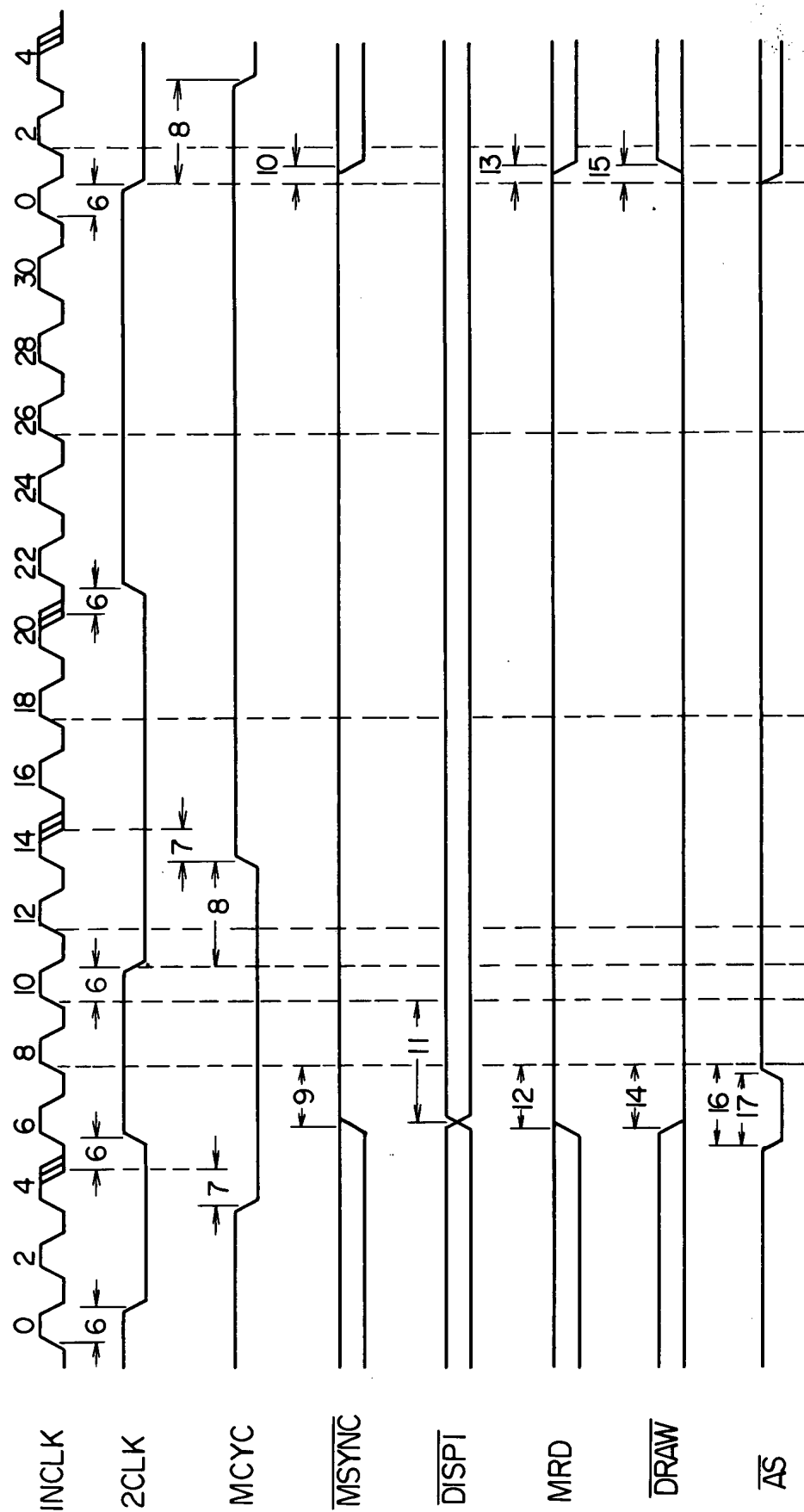




FIG. 17b

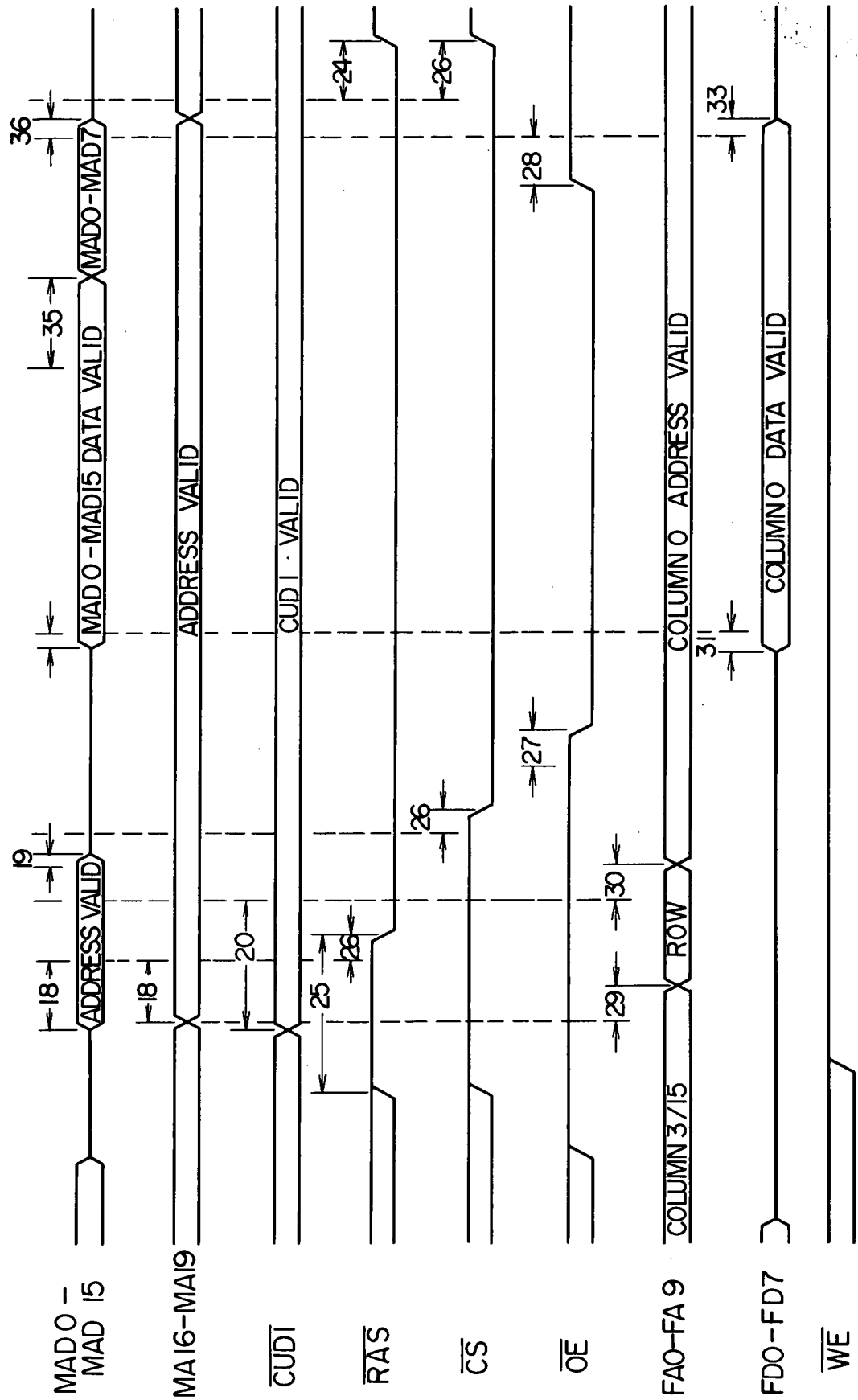


FIG. 18a

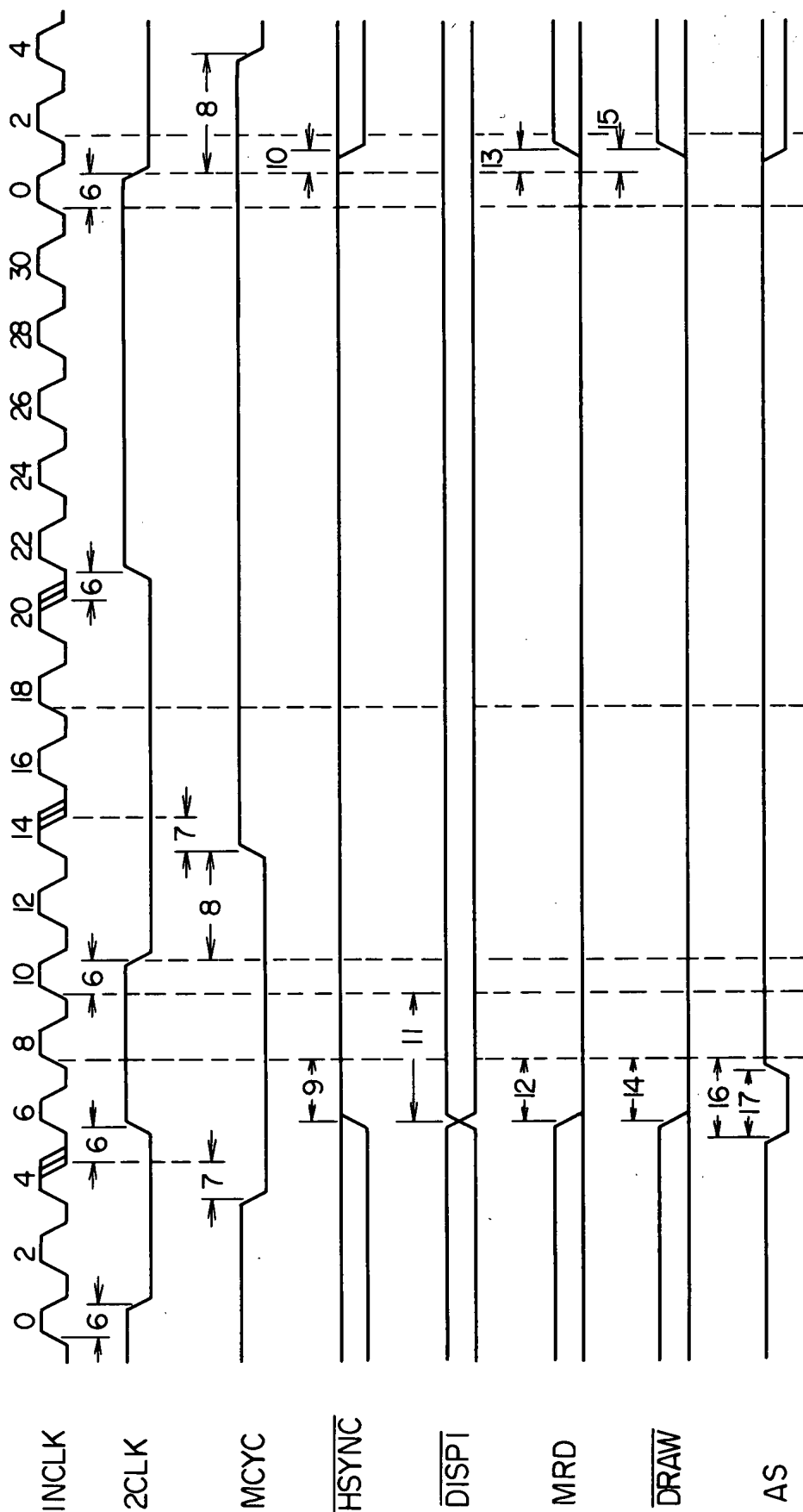


FIG. 18b

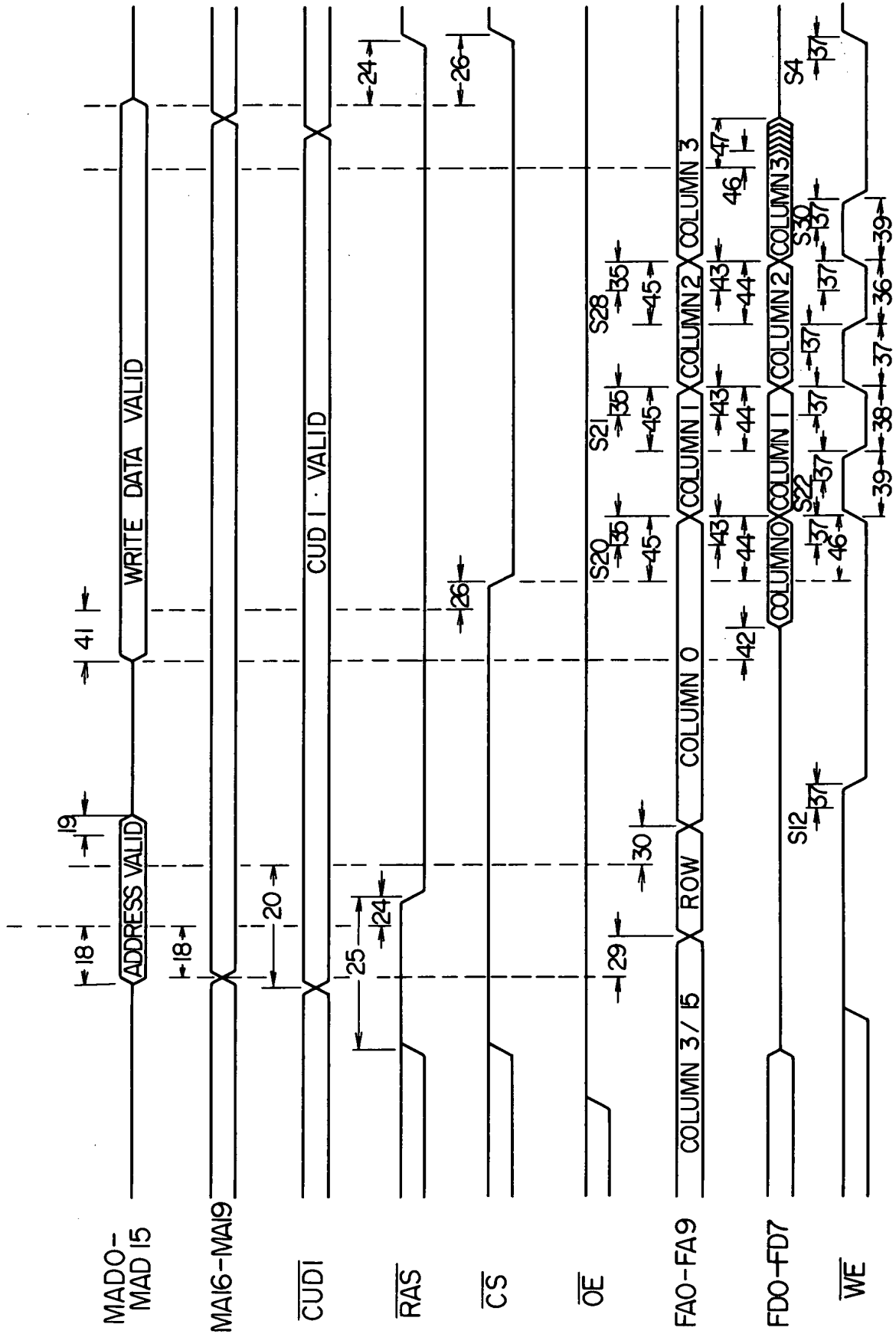
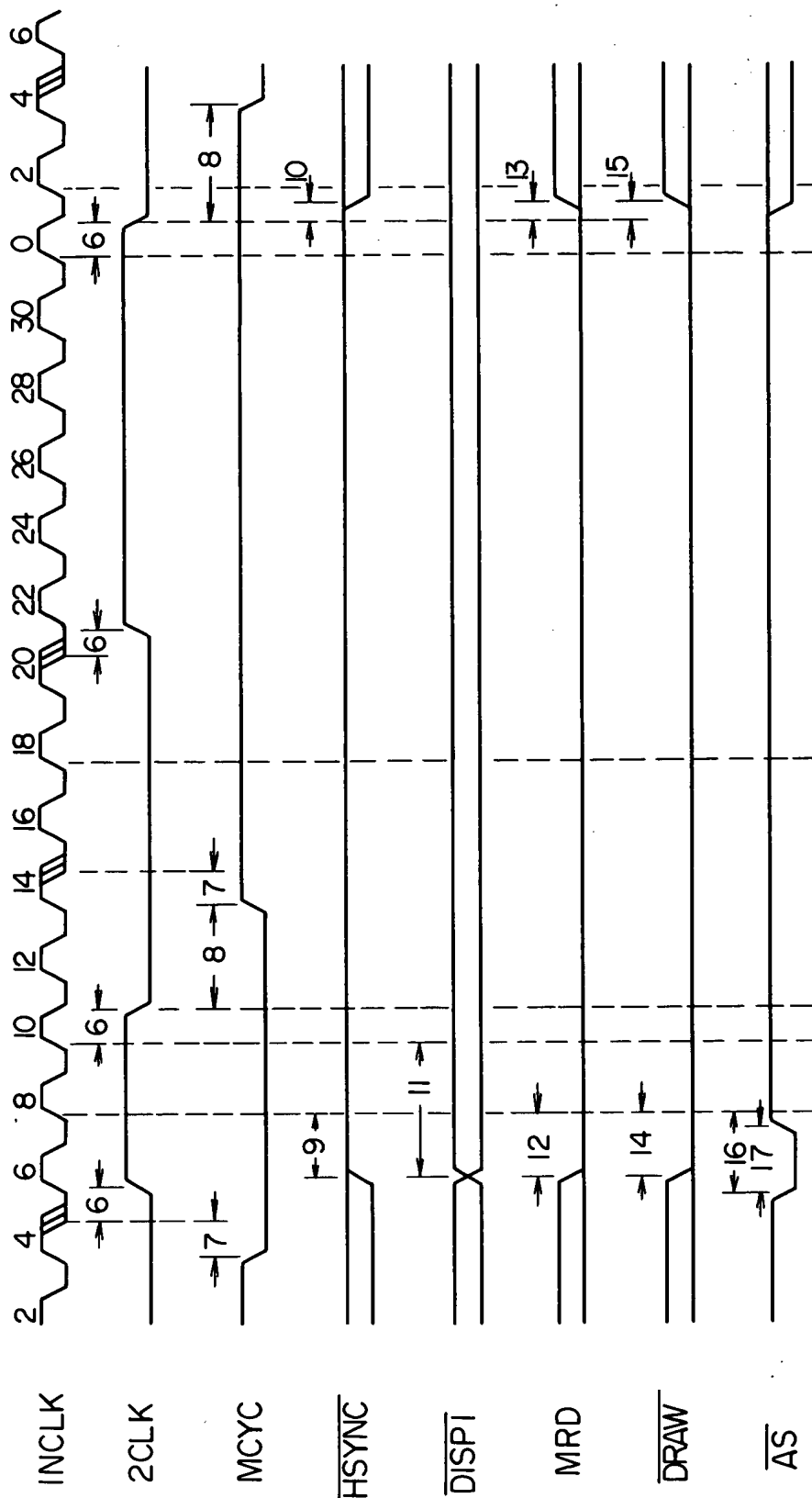


FIG. 19a



F I G. 1961

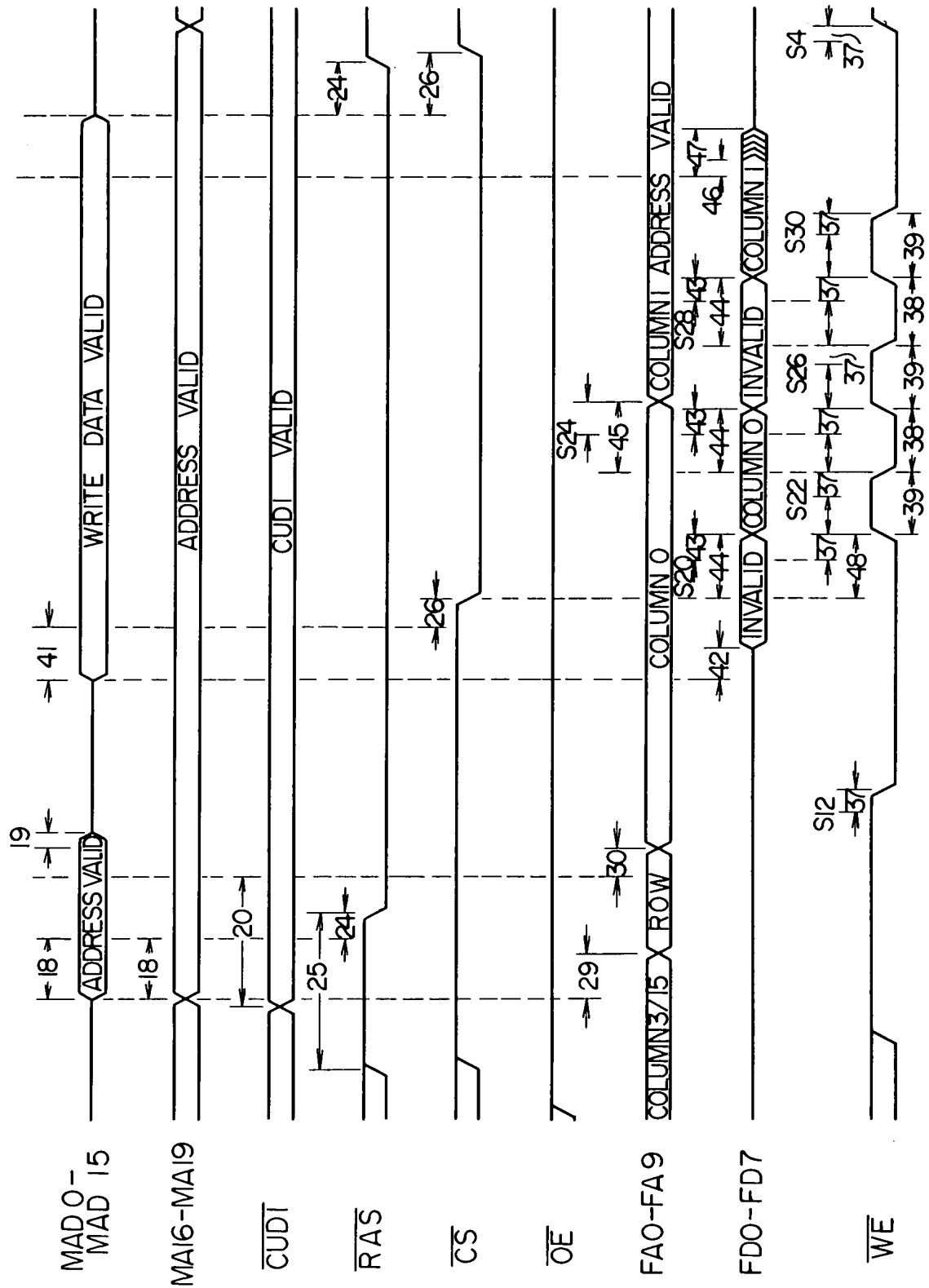


FIG. 20a

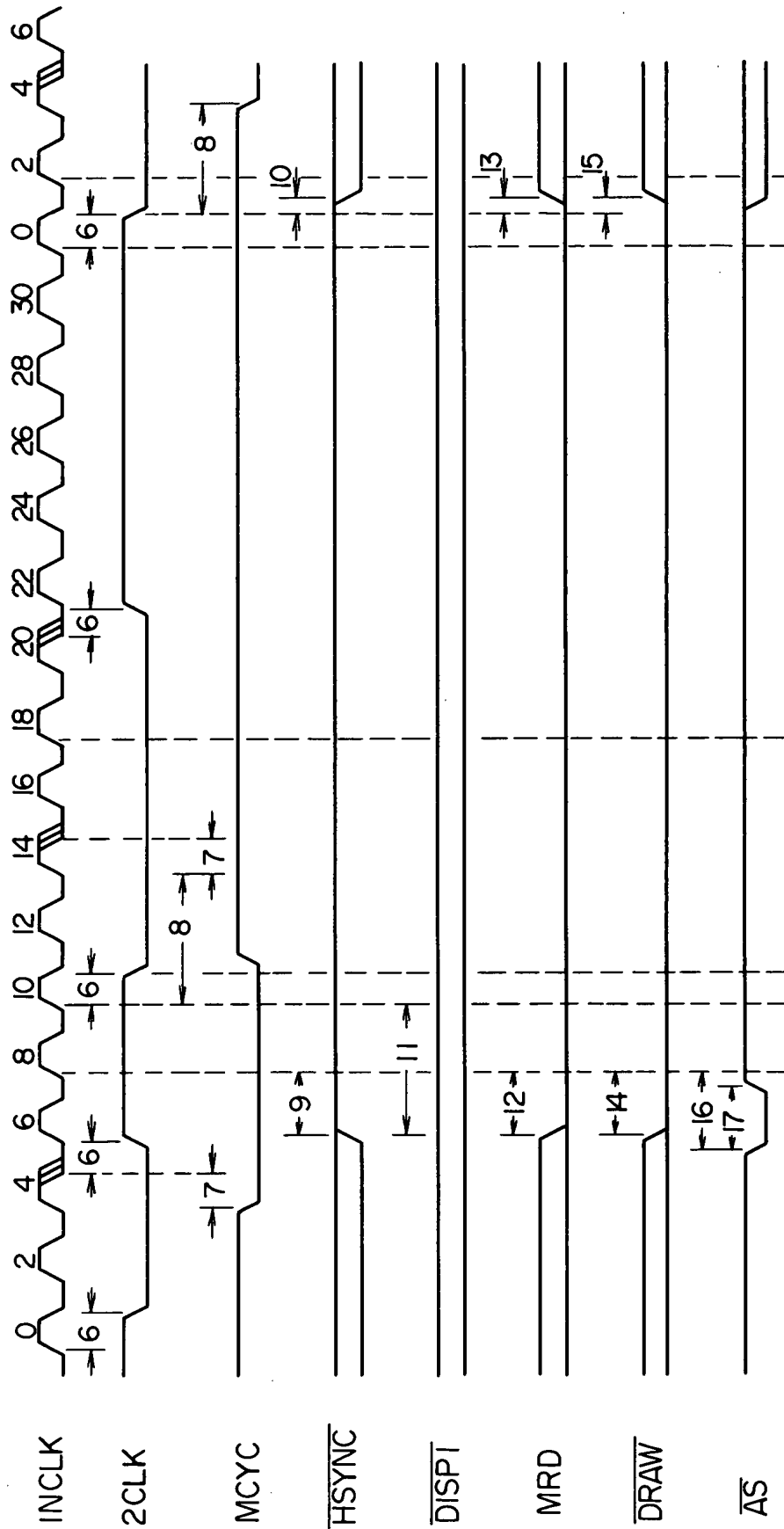


FIG. 20b

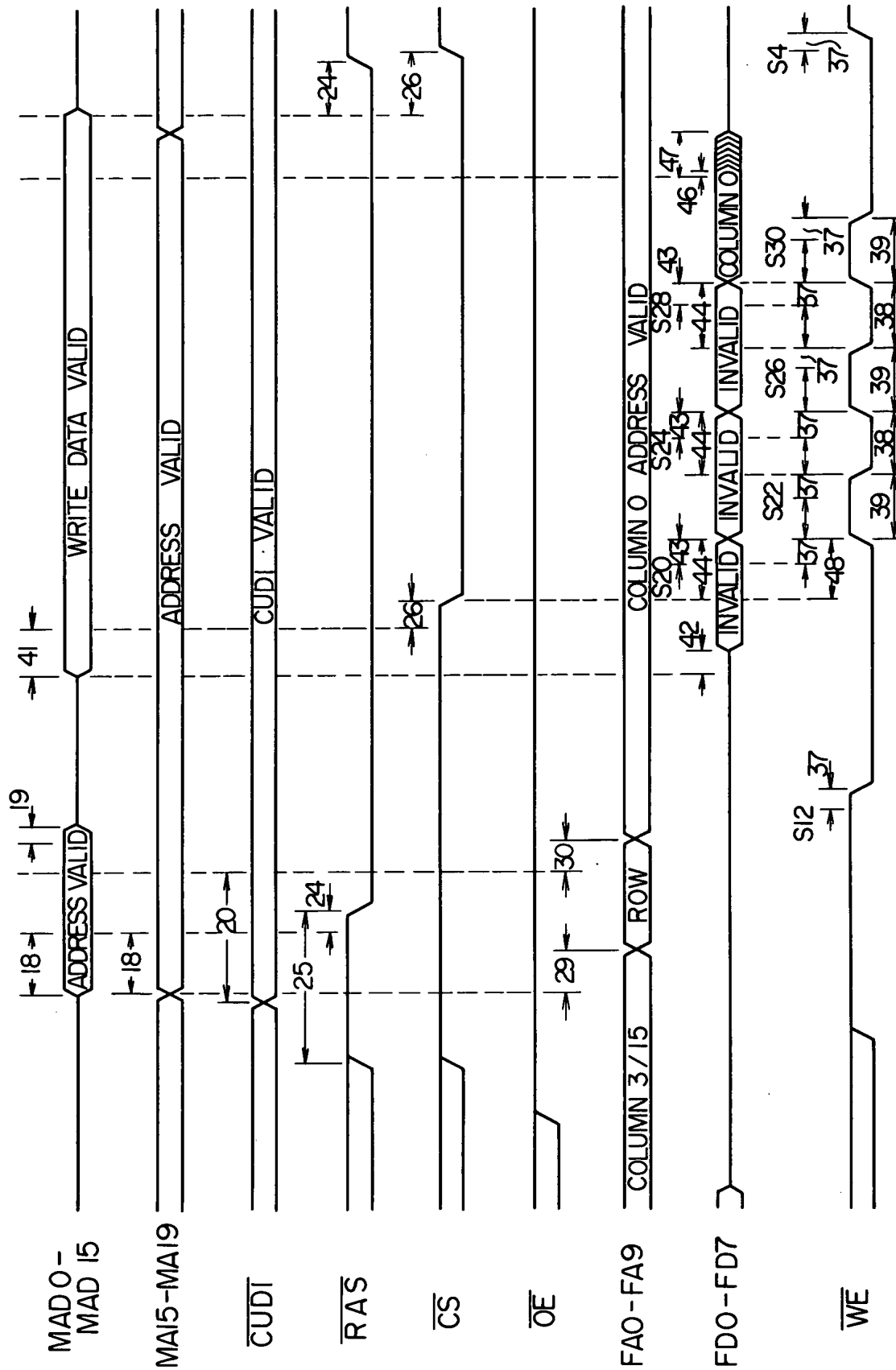
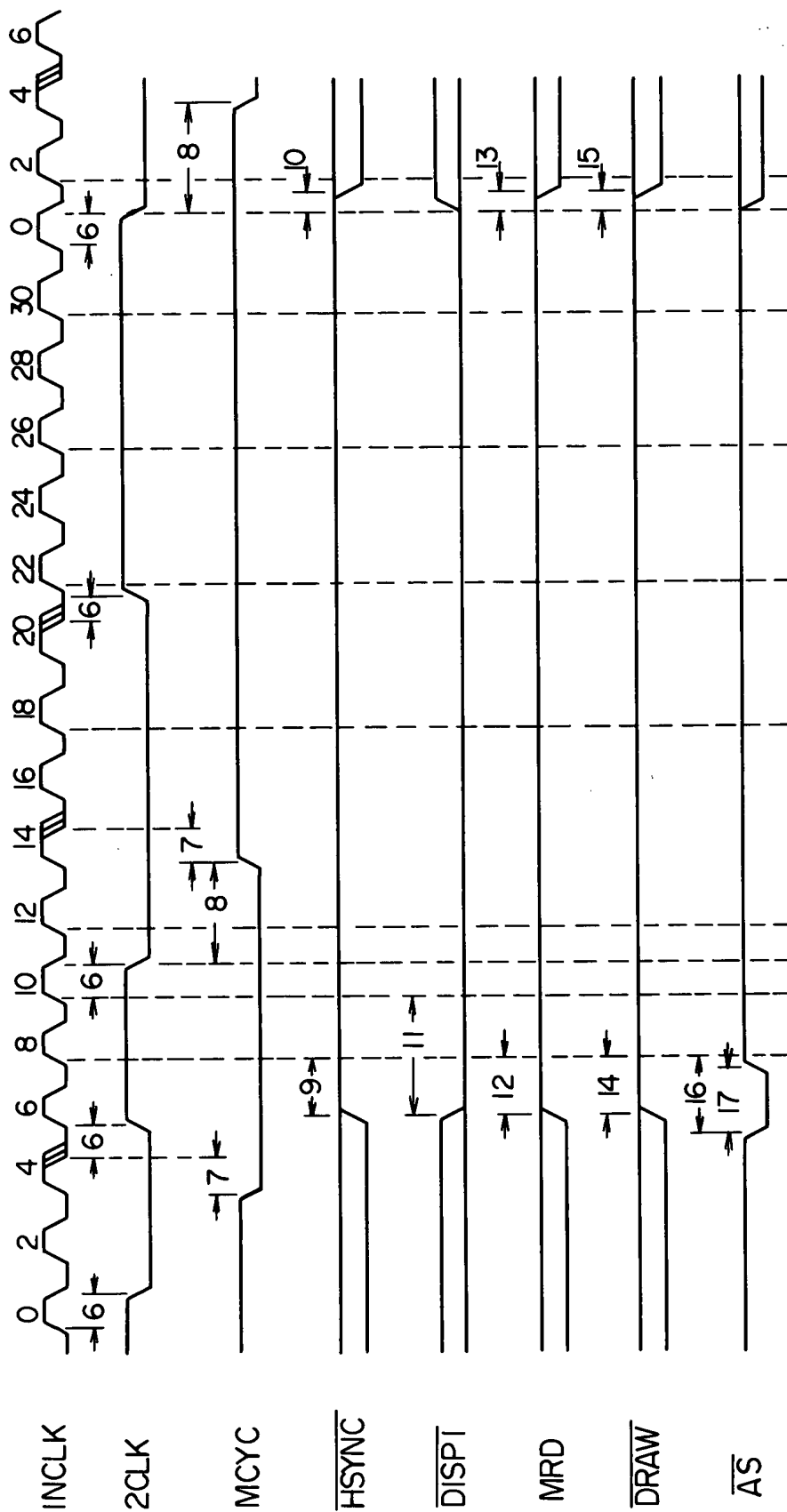


FIG. 21a





F I G. 21b

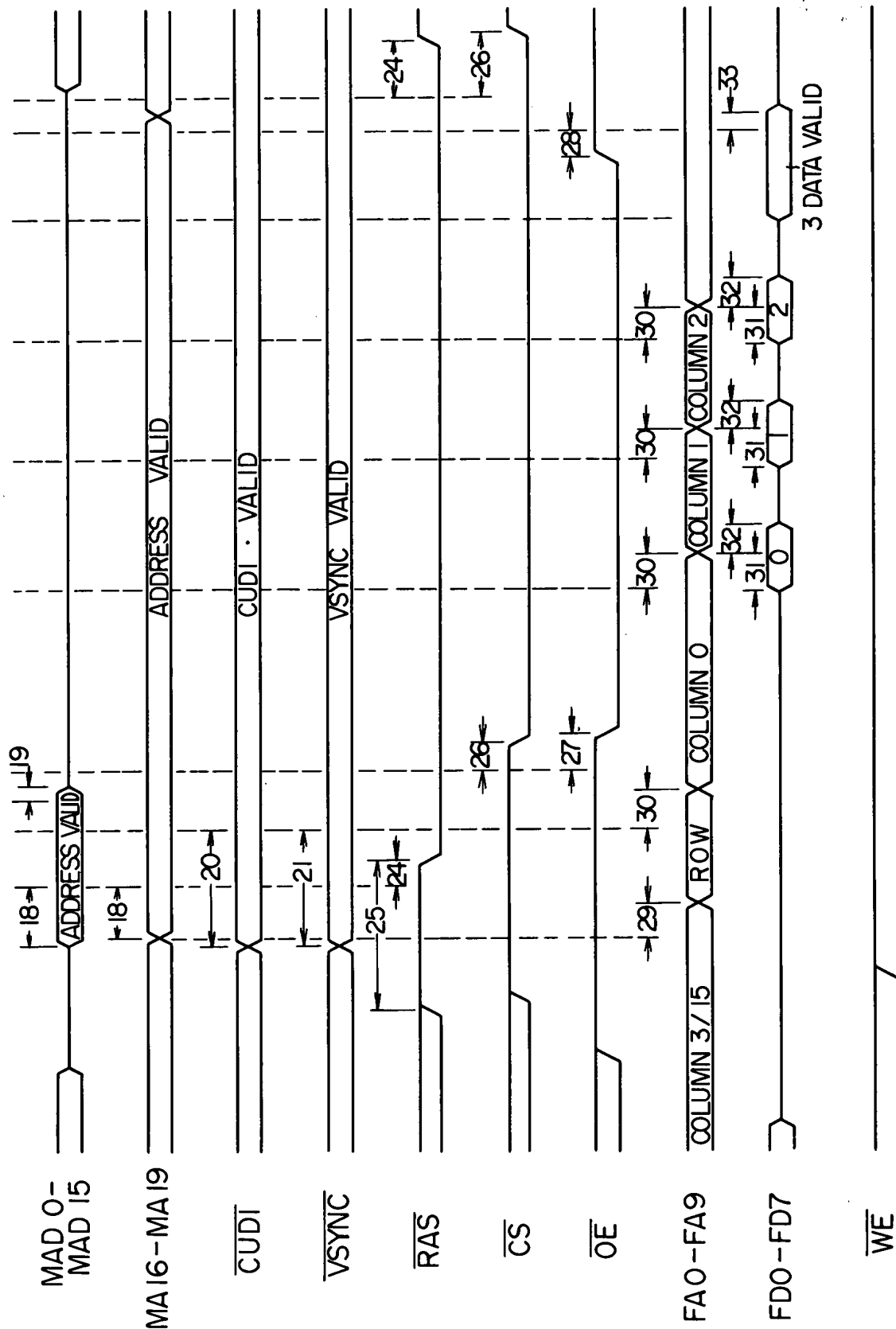


FIG. 22a

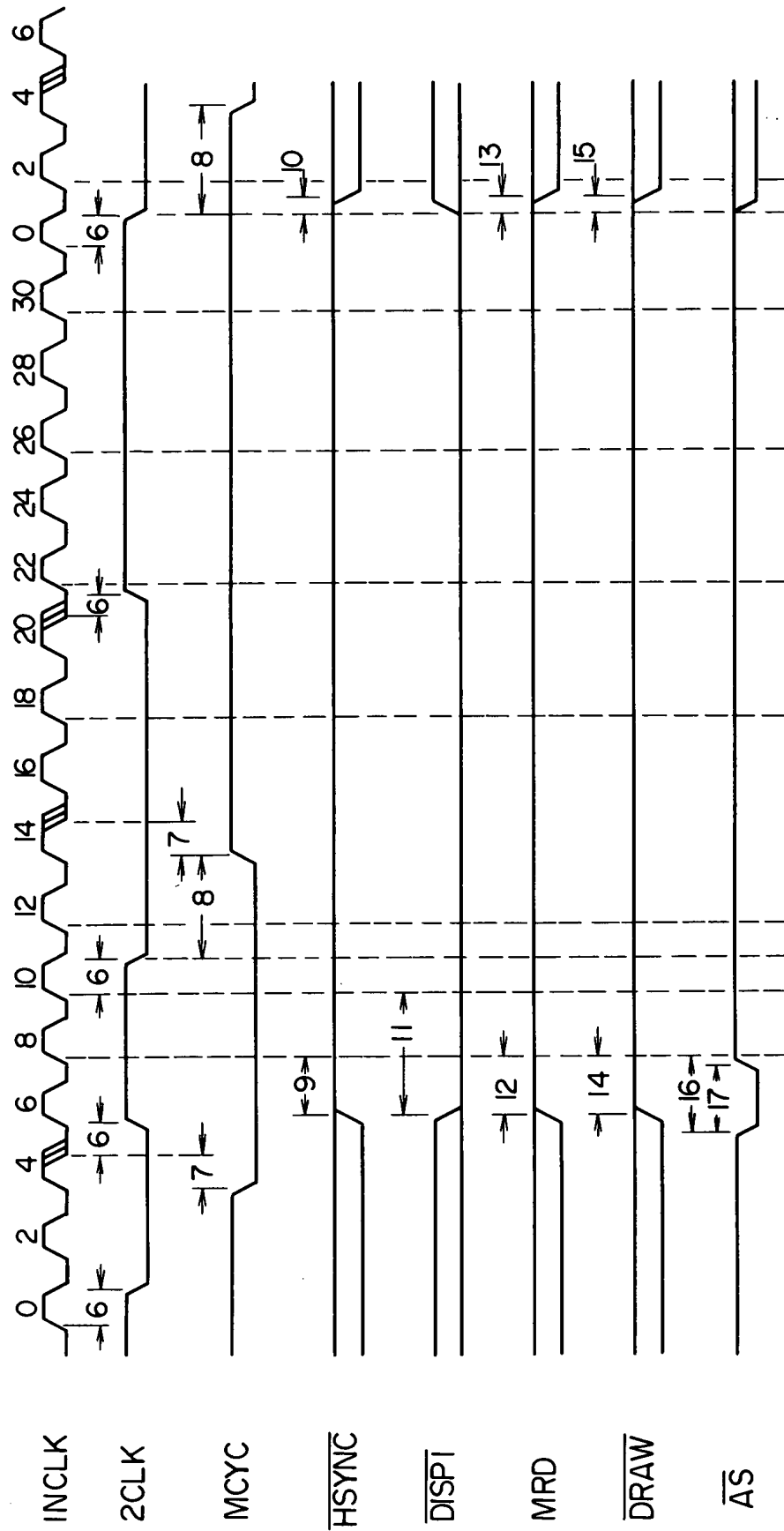
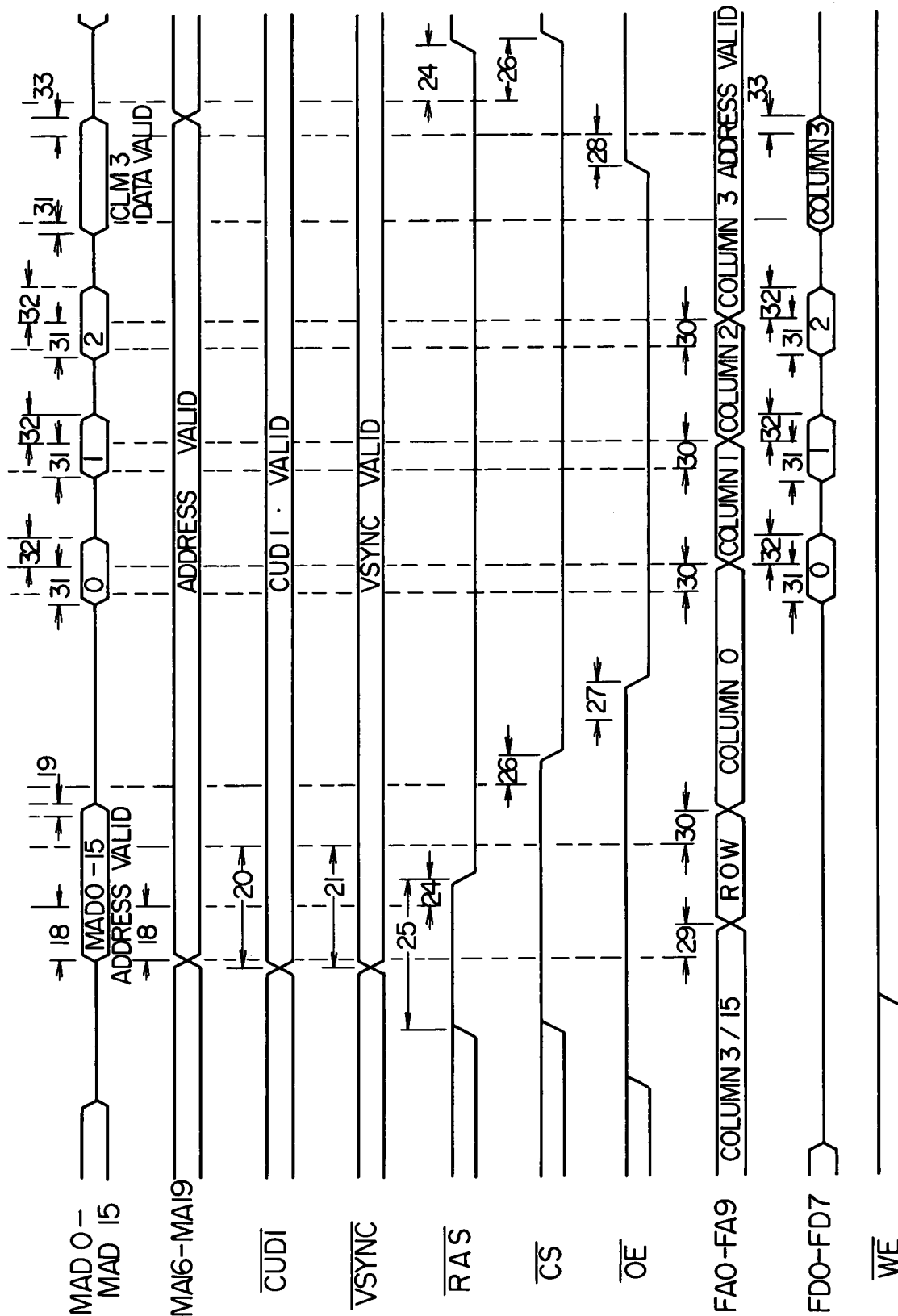


FIG. 22b



F I G. 23a

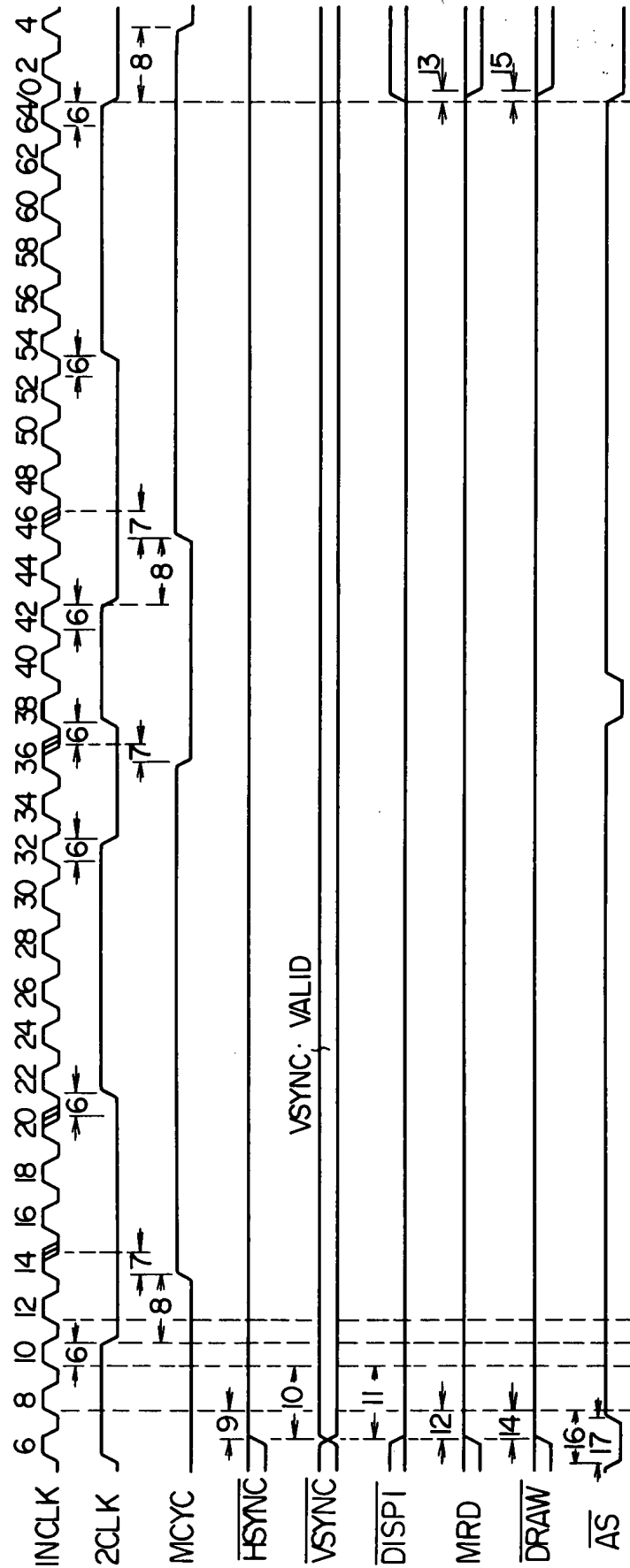


FIG. 23b

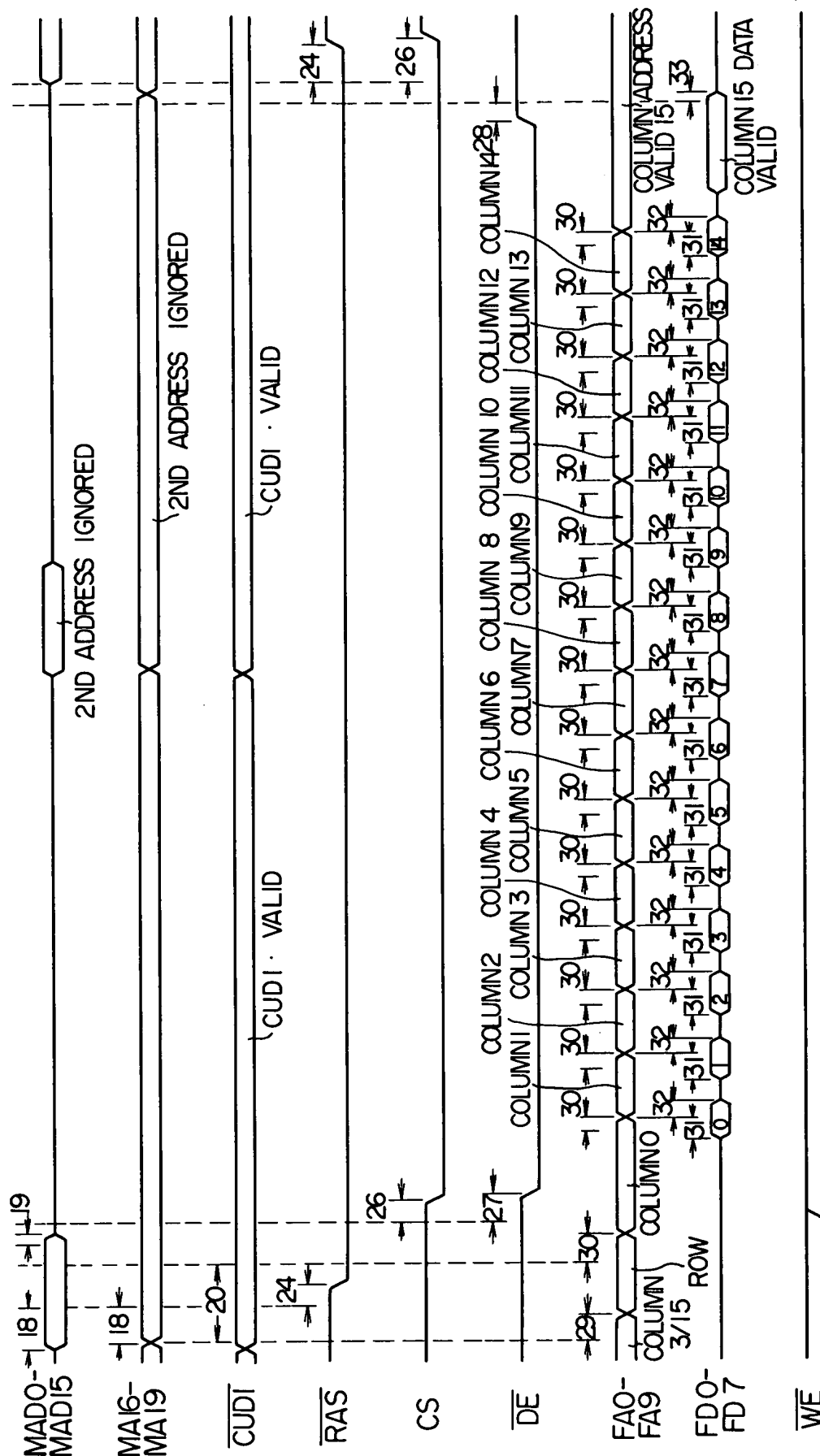


FIG. 24a

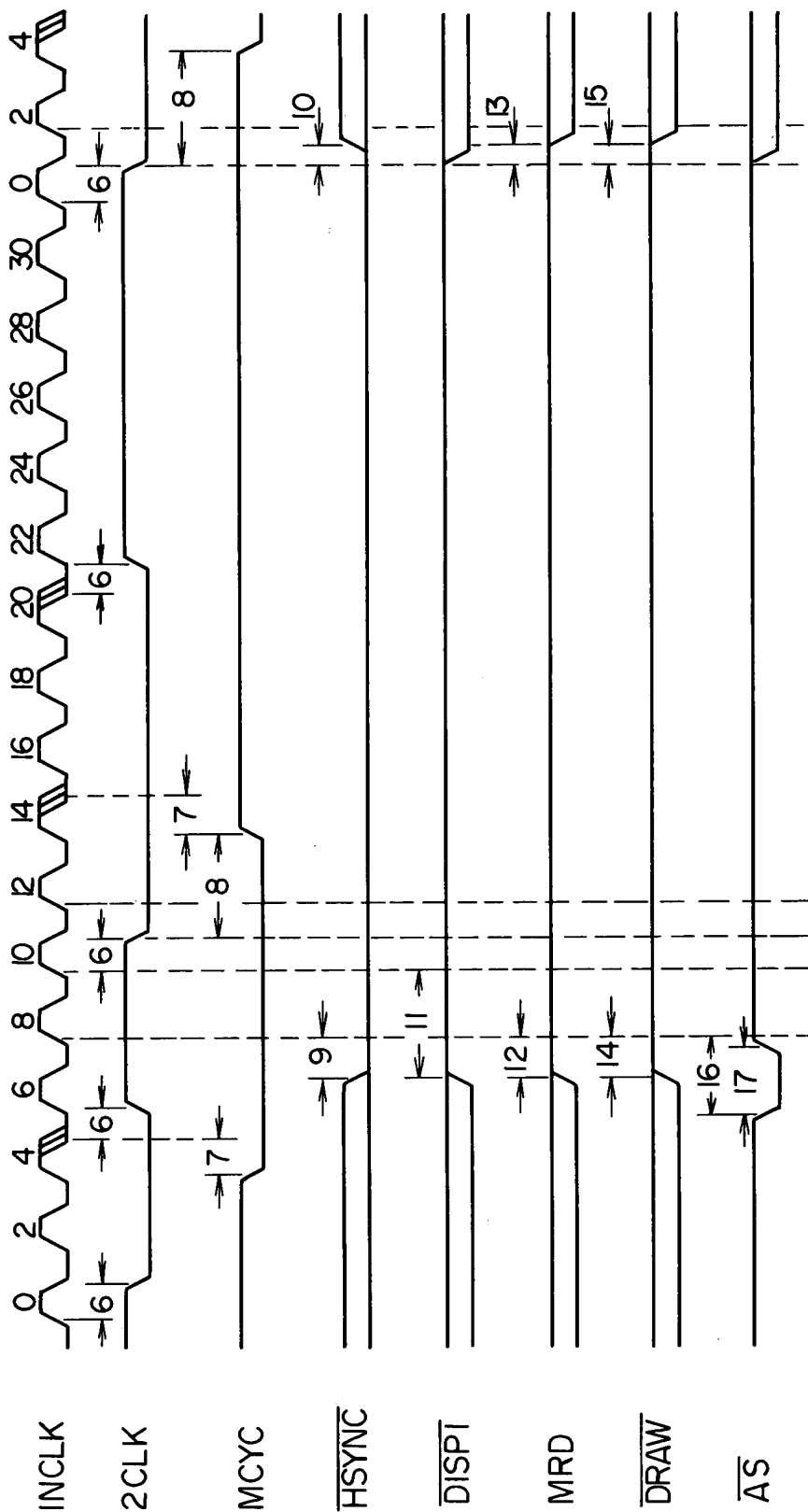
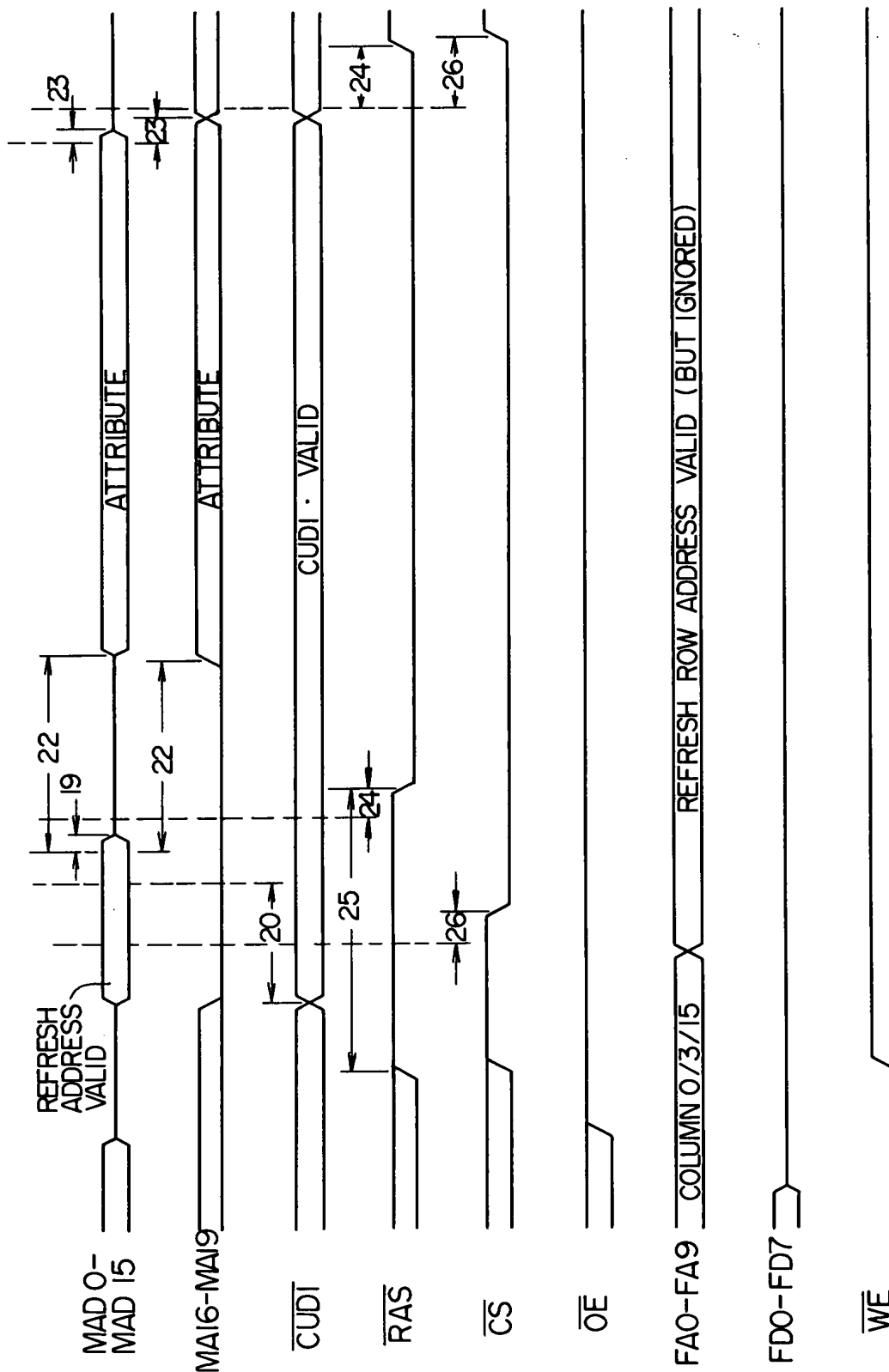
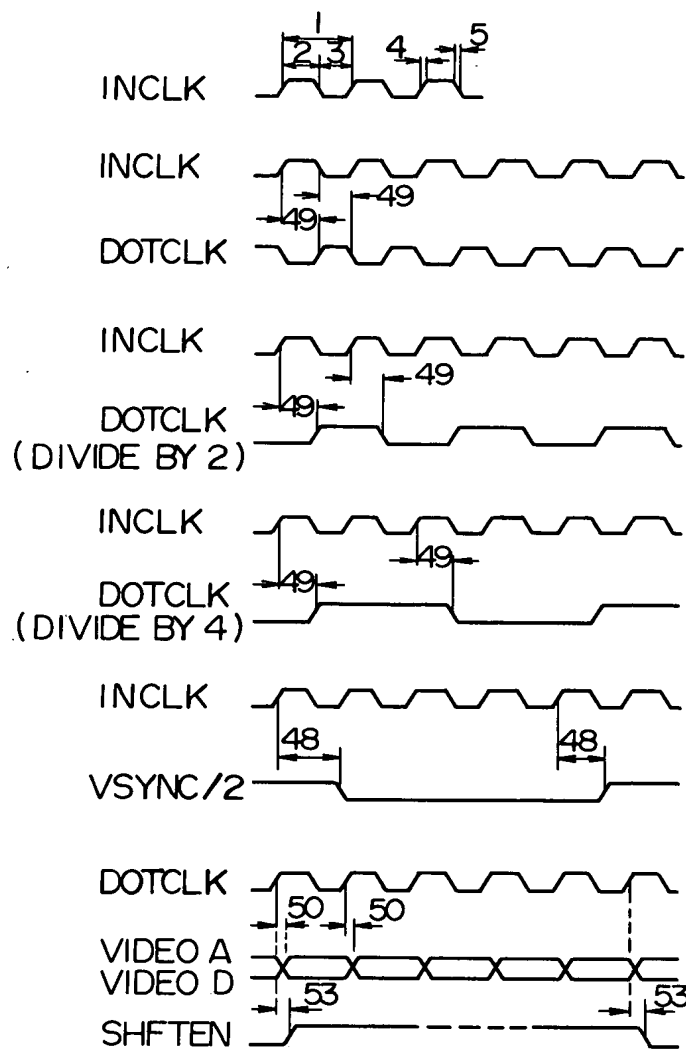


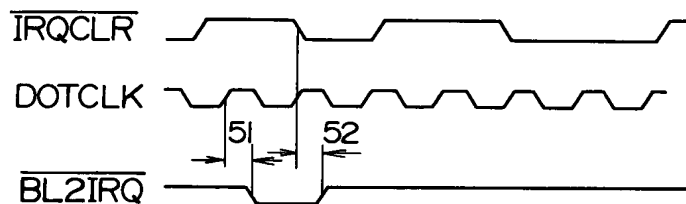
FIG. 24b



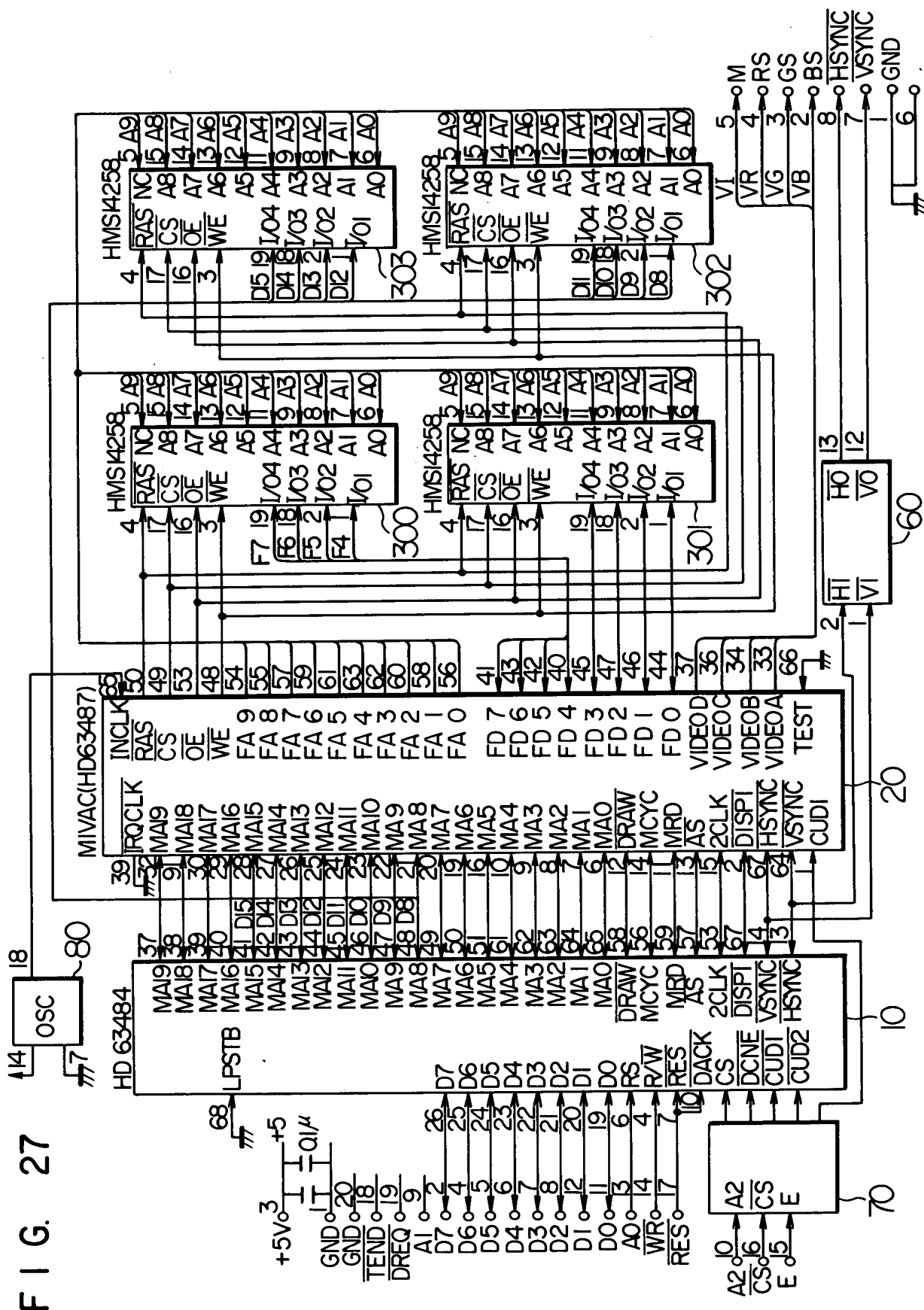
F I G. 25



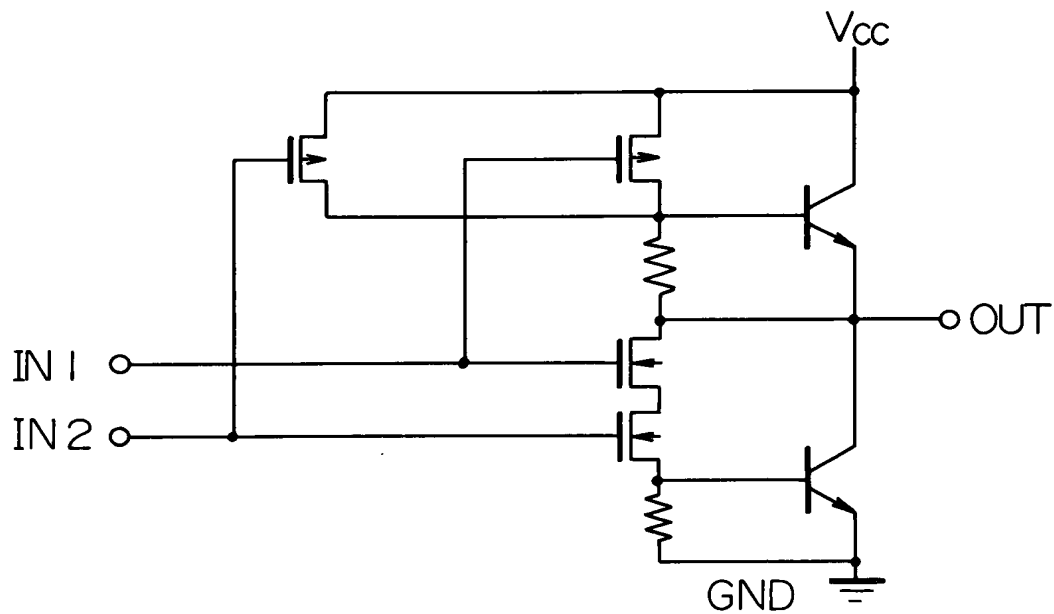
F I G. 26







F I G. 28



F I G. 29a

FA	4 ACCESSSES / MCYC (DRAW, DISPLAY)				16 ACCESSSES / 2 MCYCS (DISPLAY)			
	256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)		256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	—	—	MAD 8	NC0	—	—	MAD 8	NC0
8	MAD 9	NC1	MAD 9	NC1	MAD 9	NC1	MAD 9	NC1
7	MAD 8	NC2	MA 17	MAD 7	MAD 8	NC2	MA 17	MAD 7
6	MAD 7	MAD 6	MA 16	MAD 6	MAD 7	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC1	MAD 11	WC1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WC0	MAD 10	WC0

[ ] : COLUMN ADDRESS COUNTER

FIG. 29b

	2 ACCESSSES / MCYC ( DRAW )				4 ACCESSSES / MCYC ( DISPLAY )				16 ACCESSSES / 2MCYCS ( DISPLAY )			
	256Kx4 - BIT (VMDO=0)	1Mx4 - BIT (VMDO=1)	256Kx4 - BIT (VMDO=0)	1Mx4 - BIT (VMDO=1)	256Kx4 - BIT (VMDO=0)	1Mx4 - BIT (VMDO=1)	256Kx4 - BIT (VMDO=0)	1Mx4 - BIT (VMDO=1)	256Kx4 - BIT (VMDO=0)	1Mx4 - BIT (VMDO=1)	256Kx4 - BIT (VMDO=0)	1Mx4 - BIT (VMDO=1)
FA	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	-	-	MA 18	[NCO]	-	[NCO]	MA 18	[NCO]	-	-	MA 18	[NCO]
8	MAD 9	[NCI]	MAD 9	MAD 8	MAD 9	[NCI]	MAD 9	MAD 8	MAD 9	[NCI]	MAD 9	MAD 8
7	MAD 8	MAD 7	MA 17	MAD 7	MAD 8	MAD 7	MA 17	MAD 7	MAD 8	MAD 7	MA 17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	[WC 2]	MAD 12	[WC 2]
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	[WC 1]	MAD 11	[WC 1]
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	[WCO]	MAD 10	[WCO]	MAD 10	[WCO]	MAD 10	[WCO]

[ ] : COLUMN ADDRESS COUNTER

## F I G. 29c

FA	1 ACCESSES / MCYC ( DRAW )				4 ACCESSES / MCYC ( DISPLAY )			
	256K x 4 -BIT (VMDO=0)		1M x 4 -BIT (VMDO=1)		256K x 4-BIT (VMDO=0)		1M x 4 -BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	-	-	MA 18	MAD 9	-	-	MA 18	MAD 9
8	MAD 9	MAD 8	MA 19	MAD 8	MAD 9	MAD 8	MA 19	MAD 8
7	MA 17	MAD 7	MA 17	MAD 7	MA 17	MAD 7	MAD 17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WCI	MAD 11	WCI
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WCO	MAD 10	WCO

[ ]: COLUMN ADDRESS COUNTER